EM78P350N

8-Bit Microprocessor with OTP ROM

Product Specification

DOC. VERSION 1.0

ELAN MICROELECTRONICS CORP.

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Contents

APPENDIX

Specification Revision History

Doc. Version	Revision Description	Date
1.0	Preliminary version	2006/09/14

1 General Description

The EM78P350N is an 8-bit microprocessors designed and developed with low-power and high-speed CMOS technology. It has an on-chip 8K×13-bit Electrical One Time Programmable Read Only Memory (OTP-ROM). It provides a protection bit to prevent intrusion of user's OTP memory code. Three Code option bits are also available to meet user's requirements.

With its enhanced OTP-ROM feature, the EM78P350N provides a convenient way of developing and verifying user's programs. Moreover, this OTP device offers the advantages of easy and effective program updates, using development and programming tools. User can avail of the ELAN Writer to easily program his development code.

2 Features

- CPU configuration
  - 8K×13 bits on chip ROM
  - 144×8 bits on chip registers (SRAM)
  - 8 level stacks for subroutine nesting
  - 4 programmable Level Voltage Detector (LVD) : 4.5V, 4.0V, 3.3V, 2.2V
  - 4 programmable Level Voltage Reset (LVR) : 4.0V, 3.5V, 2.7V, 1.8V (POR)
  - Less than 2.2 mA at 5V/4MHz
  - Typically 15 μA, at 3V/32kHz
  - Typically 1 μA, during sleep mode
- I/O port configuration
  - 4 bidirectional I/O ports : P5, P6, P7, P8
  - 29 I/O pins
  - Wake-up port : P6
  - 29 Programmable pull-down I/O pins
  - 29 programmable pull-high I/O pins
  - External interrupt : P52, P53
- Operating voltage range:
  - OTP version:
    Operating voltage range: 2.1V~5.5V
  - Mask ROM version:
    Operating voltage range: 1.8V~5.5V
- Operating temperature range: -40~85°C
- Operating frequency range:
  Main clock
  - Crystal mode:
    DC ~ 20MHz/2clks @ 5V; DC ~100ns inst. cycle @ 5V
    DC ~ 8MHz/2clks @ 3V;DC ~ 250ns inst. cycle @ 3V
  - ERC mode:
    DC ~ 16MHz/2clks @ 5V; DC ~ 125ns inst. cycle @ 5V
    DC ~ 8MHz/2clks @ 3V; DC ~ 250ns inst. cycle @ 3V
  - IRC mode:
    Oscillation mode : 4MHz, 8MHz, 1MHz, 455kHz
    Process deviation : Typ±3%, Max±5%
    Temperature deviation : ±10% (-40°C~85°C)
    Sub clock
    Crystal: 32.768kHz
- Peripheral configuration
  - Serial peripheral interface (SPI) available
  - 8-bit real time clock/counter (TCC) with selective signal sources, trigger edges, and overflow interrupt
  - 8-bit channels Analog-to-Digital Converter with 12-bit resolution
  - Three Pulse Width Modulation (PWM) with 10-bit resolution
  - One pair of comparators or OP
- Eight available interrupts:
  - TCC overflow interrupt
  - Input-port status changed interrupt (wake-up from sleep mode)
  - Two External interrupt
  - ADC completion interrupt
  - PWM time period match completion interrupt
  - Comparator high/low interrupt
  - Serial I/O interrupt
  - Low voltage detect (LVD)
- Special features
  - Programmable free running watchdog timer
  - High ESD immunity
  - High EFT immunity
  - Power saving Sleep mode
  - Selectable Oscillation mode
- Package types:

28 pin DIP	600mil	EM78P350NP
28 pin SOP	300mil	EM78P350NM
28 pin SDIP	400mil	EM78P350NK
28 pin SDIP	300mil	EM78P350NAK
32 pin LQFP		EM78P351NQ
32 pin SDIP	400mil	EM78P351NK
32 pin DIP	600mil	EM78P351NP
32 pin SOP I	300mil	EM78P351NM

3 Pin Assignment

(1) 28-Pin DIP/SOP

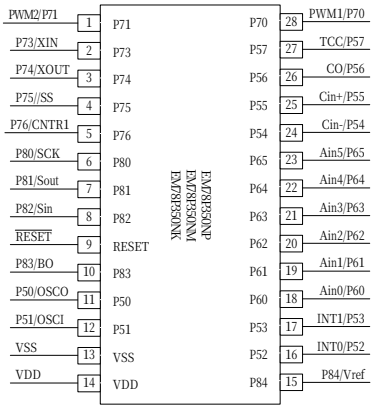


Fig. 3-1 28-pin DIP/SOP

(2) 32-Pin QFP

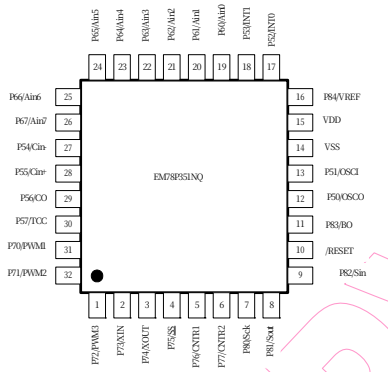


Fig. 3-2 32-pin QFP

(3) 32-Pin SOP/SDIP/DIP

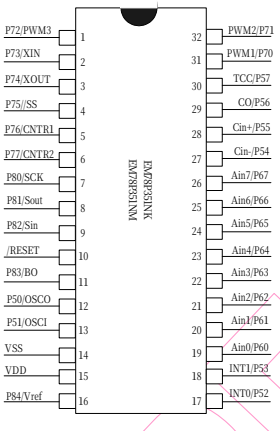


Fig. 3-1 32-pin DIP/SOP

4 Functional Block Diagram

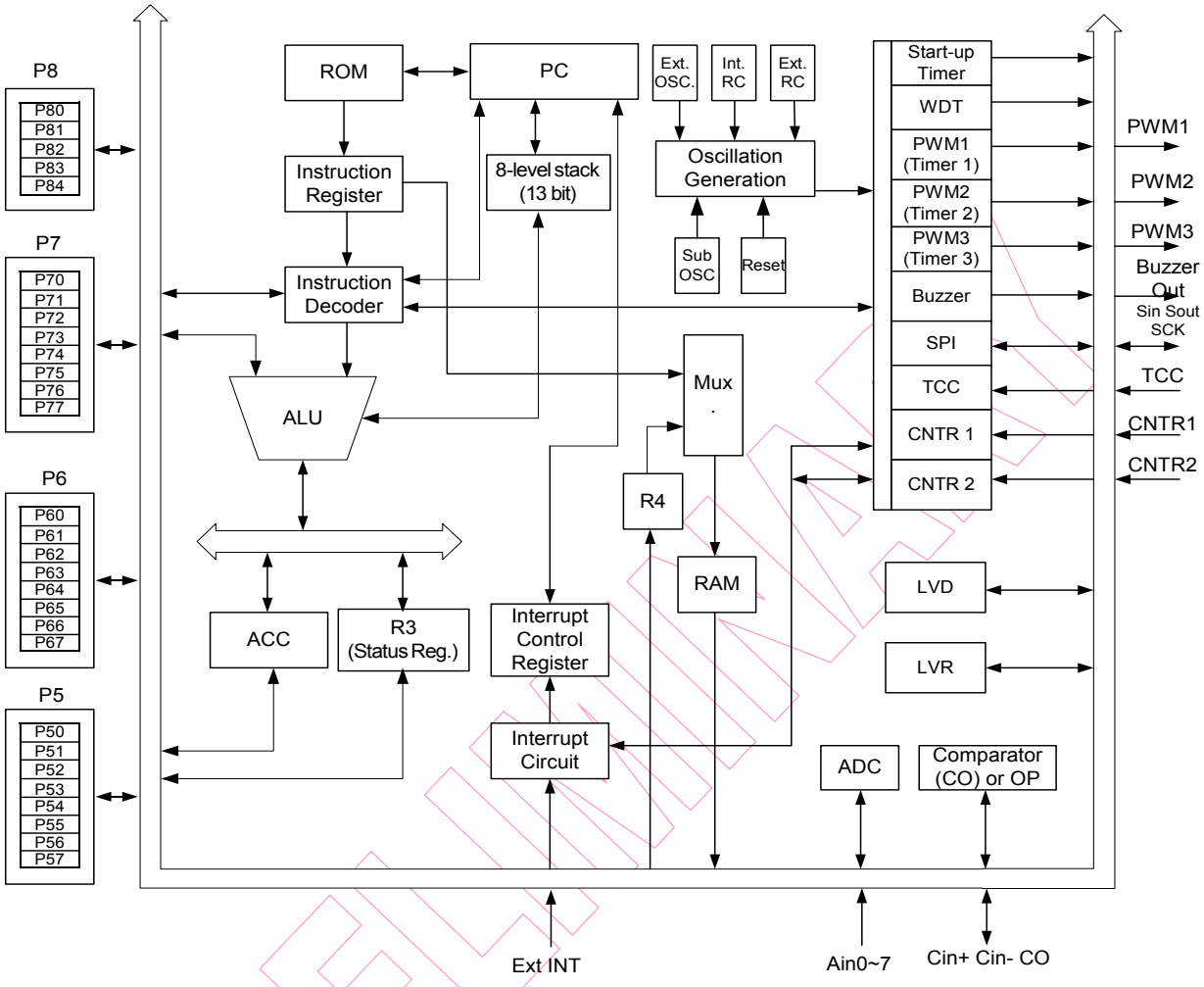


Fig. 4-1 EM78P350N Functional Block Diagram

5 Pin Description

5.1 EM78P350

Symbol	Pin No.	Type	Function
P50~P57	11~12 16~17 24~27	I/O	8-bit General purpose input/output pins Default value at power-on reset
P60~P65	18~23	I/O	6-bit General purpose input/output pins Default value at power-on reset
P70~P71 P73~P76	28, 1 2~5	I/O	6-bit General purpose input/output pins Default value at power-on reset
P80 ~ P84	6~8 10, 15	I/O	5-bit General purpose input/output pins Default value at power-on reset
INT0, INT1	16, 17	I	External interrupt pin triggered by falling edge
Ain0~Ain5	18~22	I	6-bit Analog-to-Digital Converter Defined by AISR (Bank 2 R8) <0 : 7>
PWM1 PWM2	28 1	O	Pulse width modulation outputs Defined by PWMCON (Bank 1-R5)<5 : 7>
BO	10	O	Buzzer output driver
VREF	15	I	External reference voltage for ADC Defined by ADCON (Bank 2 R9) <7>.
CIN- CIN+ CO	24 25 26	I I O	"-" : the input pin of Vin- of the comparator "+" : the input pin of Vin+ of the comparator Pin CO is the comparator output Defined by CMPCON (IOCA) <0:1>
/RESET	9	I	General-purpose Input only If it remains at logic low, the device will be reset Wake-up from sleep mode when pin status changes Voltage on /RESET must not exceed Vdd during normal mode
TCC	27	I	Real time clock/counter with Schmitt Trigger input pin. It must be tied to VDD or VSS if not in use.
CNTR1	5	I	Counter 1 / Counter 2 with Schmitt Trigger input pin.
Sin	8	I	Sin pin is used to input serial data signals by software. Sin pin is also used as port P82.
Sout	7	O	Sout pin is used to input serial data signals by software. Sout pin is also used as port P81.
Sck	6	I/O	Sck pin is used to input and output synchronous clock signals for serial data transfer by software. Sck pin is also used as Port P80.
OSCI	12	I	Crystal type: Crystal input terminal or external clock input pin RC type: RC oscillator input pin
OSCO	11	O	Crystal type: Output terminal for crystal oscillator or external clock input pin. RC type: Clock output with a duration of one instruction cycle time. The prescaler is determined by the CONT register. External clock signal input.
XIN	2	I	Low crystal 32.768kHz input
XOUT	3	O	Low crystal 32.768kHz output
VDD	14	–	Power supply
VSS	13	–	Ground

5.2 EM78P351

Symbol	Pin No.	Type	Function
P50~P57	12~13 17~18 27~30	I/O	8-bit General purpose input/output pins Default value at power-on reset
P60~P67	19~26	I/O	8-bit General purpose input/output pins Default value at power-on reset
P70~P77	31~32 1~6	I/O	8-bit General purpose input/output pins Default value at power-on reset
P80 ~ P84	7~9 11, 16	I/O	5-bit General purpose input/output pins Default value at power-on reset
INT0, INT1	17, 18	I	External interrupt pin triggered by falling edge
Ain0~Ain7	19~26	I	8-bit Analog-to-Digital Converter Defined by AISR (Bank 2 R8) <0 : 7>
PWM1 PWM2 PWM3	31 32 1	O	Pulse width modulation outputs Defined by PWMCON (Bank 1-R5)<5 : 7>
BO	11	O	Buzzer output driver
VREF	16	I	External reference voltage for ADC Defined by ADCON (Bank 2 R9) <7>.
CIN- CIN+ CO	27 28 29	I I O	"-" : the input pin of Vin- of the comparator "+" : the input pin of Vin+ of the comparator Pin CO is the comparator output Defined by CMPCON (IOCA) <0:1>
/RESET	10	I	General-purpose Input only If it remains at logic low, the device will be reset Wake-up from sleep mode when pin status changes Voltage on /RESET must not exceed Vdd during normal mode
TCC	30	I	Real time clock/counter with Schmitt Trigger input pin. It must be tied to VDD or VSS if not in use.
CNTR1/ CNTR2	5 6	I	Counter 1 / Counter 2 with Schmitt Trigger input pin.
Sin	9	I	Sin pin is used to input serial data signals by software. Sin pin is also used as Port P82.
Sout	8	O	Sout pin is used to input serial data signals by software. Sout pin is also used as Port P81.
Sck	7	I/O	Sck pin is used to input and output synchronous clock signals for serial data transfer by software. Sck pin is also used as Port P80.
OSCI	13	I	Crystal type: Crystal input terminal or external clock input pin RC type: RC oscillator input pin
OSCO	12	O	Crystal type: Output terminal for crystal oscillator or external clock input pin. RC type: Clock output with a duration of one instruction cycle time. The prescaler is determined by the CONT register. External clock signal input.
XIN	2	I	Low crystal 32.768kHz input
XOUT	3	O	Low crystal 32.768kHz output
VDD	15	–	Power supply
VSS	13	–	Ground

6 Function Description

6.1 Operational Registers

6.1.1 R0 (Indirect Address Register)

R0 is not a physically implemented register. Its major function is to perform as an indirect address pointer. Any instruction using R0 as a pointer, actually accesses the data pointed by the RAM Select Register (R4).

6.1.2 R1 (Time Clock/Counter)

- Incremented by an external signal edge through the TCC pin, or by the instruction cycle clock.
- External signal of TCC trigger pulse width must be greater than one instruction.
- The signals to increment the counter are determined by Bit 4 and Bit 5 of the CONT register.
- Writable and readable as any other registers.

6.1.3 R2 (Program Counter) and Stack

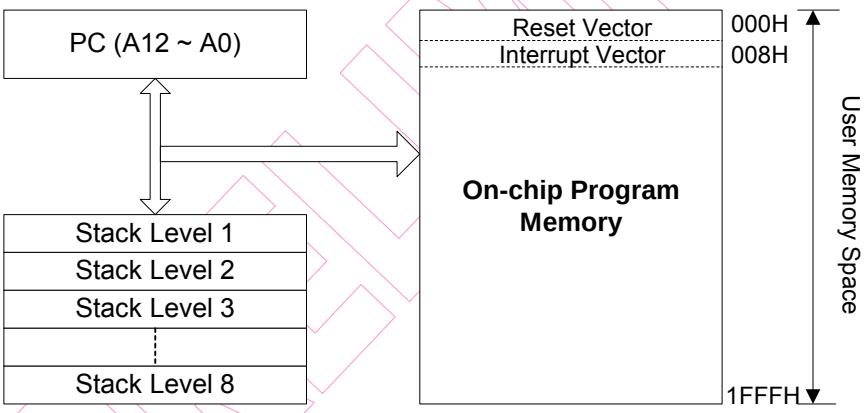
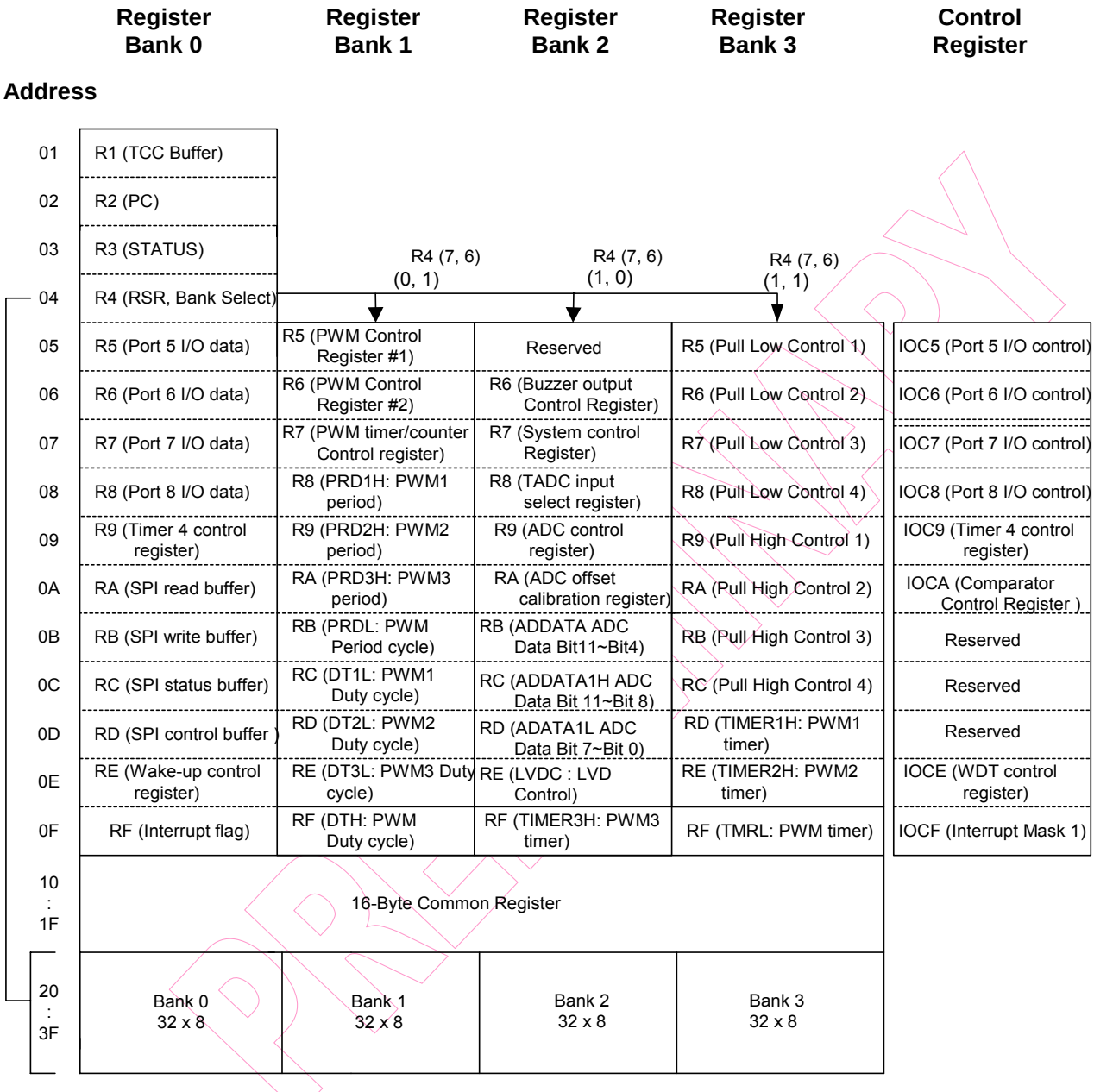


Fig. 6-1 Program Counter Organization

- R2 and hardware stacks are 12-bit wide. The structure is depicted in the table under Section 6.1.3.1 *Data Memory Configuration* (next section).
- Generates 8K×13 bits on-chip ROM addresses to the relative programming instruction codes. One program page is 1024 words long.
- The contents of R2 are all set to "0"s when a RESET condition occurs.
- "JMP" instruction allows direct loading of the lower 10 program counter bits. Thus, "JMP" allows PC to jump to any location within a page.

- "CALL" instruction loads the lower 10 bits of the PC, and then PC+1 is pushed onto the stack. Thus, the subroutine entry address can be located anywhere within a page.
- "RET" ("RETL k", "RETI") instruction loads the program counter with the contents of the top of stack.
- "ADD R2, A" allows a relative address to be added to the current PC, and the ninth and above bits of the PC will increase progressively.
- "MOV R2, A" allows loading of an address from the "A" register to the lower 8 bits of the PC, and the ninth and tenth bits (A8 ~ A9) of the PC will remain unchanged.
- Any instruction (except “ADD R2,A”) that is written to R2 (e.g., "MOV R2, A", "BC R2, 6",·····) will cause the ninth bit and the tenth bit (A8 ~ A9) of the PC to remain unchanged.
- In the case of EM78P350N, the most three significant bits (A12,A11 and A10) will be loaded with the content of PS2,PS1 and PS0 in the status register (R3) upon execution of a "JMP", "CALL", or any other instructions set which write to R2.
- All instructions are single instruction cycle (fclk/2 or fclk/4) except for the instructions that are written to R2. Note that these instructions need one or two instructions cycle as determined by Code Option Register CYES bit.

6.1.3.1 Data Memory Configuration



6.1.4 R3 (Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PS2	PS1	PS0	T	P	Z	DC	C

Bits 7 ~ 5 (PS2 ~ PS0) Page select bits. PS2~PS0 are used to pre-select a program memory page. When executing a "JMP", "CALL", or other instructions which causes the program counter to change (e.g. MOV R2, A), PS2~PS0 are loaded into the 11th,12th and 13th bits of the program counter and select one of the available program memory pages. Note that RET (RETL, RETI) instruction does not change the PS2~PS0 bits. That is, the return will always be to the page from where the subroutine was called, regardless of the PS2~PS0 bits current setting.

PS2	PS1	PS0	Program Memory Page [Address]
0	0	0	Page 0 [0000-03FF]
0	0	1	Page 1 [0400-07FF]
0	1	0	Page 2 [0800-0BFF]
0	1	1	Page 3 [0C00-0FFF]
1	0	0	Page 4 [1000-13FF]
1	0	1	Page 5 [1400-17FF]
1	1	0	Page 6 [1800-1BFF]
1	1	1	Page 7 [1C00-1FFF]

Bit 4 (T): Time-out bit. Set to 1 by the "SLEP" and "WDTC" commands or during power on and reset to 0 by WDT time-out.

Bit 3 (P): Power-down bit. Set to 1 during power-on or by a "WDTC" command and reset to 0 by a "SLEP" command.

NOTE

Bit 4 & Bit 3 (T & P) are read only.

Bit 2 (Z): Zero flag. Set to "1" if the result of an arithmetic or logic operation is zero.

Bit 1 (DC): Auxiliary carry flag

Bit 0 (C): Carry flag

6.1.5 R4 (RAM Select Register)

Bit 7 & Bit 6: are used to select Banks 0 ~ 3.

Bit 5 ~ Bit 0: are used to select registers (address: 00 ~ 3F) in the indirect address mode.

See the table under Section 6.1.3.1 *Data Memory Configuration* for the configuration of the data memory.

6.1.6 R5 ~ R8 (Port 5 ~ Port 8)

R5 ~ R7 are I/O registers.

R8 is an I/O register. The upper 3 bits of R8 are fixed to 0.

6.1.7 R9 (TMR4: Timer 4 Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TMR47	TMR46	TMR45	TMR44	TMR43	TMR42	TMR41	TMR40

TMR47~TMR40 are set of Timer 4 register bits which are incremented until the value matches PWP and then, it resets to 0.

6.1.8 RA (SPIRB: SPI Read Buffer)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SRB7	SRB6	SRB5	SRB4	SRB3	SRB2	SRB1	SRB0

SRB7~SRB0 are 8-bit data when transmission is completed by SPI.

6.1.9 RB (SPIWB: SPI Write Buffer)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SWB7	SWB6	SWB5	SWB4	SWB3	SWB2	SWB1	SWB0

SWB7~SWB0 are 8-bit data, waiting for transmission by SPI.

6.1.10 RC (SPIS: SPI Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DORD	TD1	TD0	T4ROS	OD3	OD4	-	RBF

Bit 7 (DORD): Data transmission order.

0 :Shift left (MSB first)

1 :Shift right (LSB first)

Bit 6~Bit 5: Sout Status output Delay times Options

TD1	TD0	Delay Time
0	0	8 CLK
0	1	16 CLK
1	0	24 CLK
1	1	32 CLK

Bit 4 (T4ROS): Timer4 Read Out Buffer Select Bit

0 : Read Value from Timer 4 Preset Register.

1 : Read Value from Timer 4 Counter Register.

Bit 3 (OD3): Open-Drain Control bit

0 = Open-drain disable for Sout

1 = Open-drain enable for Sout

Bit 2 (OD4): Open-Drain Control bit

0 = Open-drain disable for SCK

1 = Open-drain enable for SCK

Bit 1 are not used and read as "0".

Bit 0 (RBF): Read Buffer Full flag

0 = Receiving not completed, and SPIRB has not fully exchanged. When users read SPIRB, RBF bit will be cleared.

1 = Receiving completed; SPIRB is fully exchanged.

6.1.11 RD (SPIC: SPI Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CES	SPIE	SRO	SSE	SDOC	SBRS2	SBRS1	SBRS0

Bit 7 (CES): Clock Edge Select bit

0 = Data shifts out on a rising edge, and shifts in on a falling edge. Data is on hold during a low-level.

1 = Data shifts out on a falling edge, and shifts in on a rising edge. Data is on hold during a high-level.

Bit 6 (SPIE): SPI Enable bit

0 = Disable SPI mode

1 = Enable SPI mode

Bit 5 (SRO): SPI Read Overflow bit

0 = No overflow

1 = A new data is received while the previous data is still being held in the SPIB register. In this situation, the data in SPIS register will be destroyed. To avoid setting this bit, users are required to read the SPIRB register although only the transmission is implemented.

NOTE

This can only occur in slave mode.

Bit 4 (SSE): SPI Shift Enable bit

0 = Reset as soon as the shifting is completed, and the next byte is ready to shift.

1 = Start to shift, and remain on "1" while the current byte is still being transmitted.

NOTE

This bit will reset to 0 at every one-byte transmission by the hardware

Bit 3 (SOUTC): Sout output status control bit:

0 = After the Serial data output, the Sout remains high

1 = After the Serial data output, the Sout remains low

Bit 2~Bit 0 (SBRS): SPI Baud Rate Select bits

Refer to the SPI baud rate table under the "SPI" section on the subsequent pages.

6.1.12 RE (WUCR: Wake-up Control Register)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EM78P350N	"0"	"0"	"0"	LVDIF*	ADWE	CMPWE	ICWE	PWMWE
ICE350N Simulator	C3	C2	C1	C0	ADWE	CMPWE	ICWE	PWMWE

***There is no LVD function in the ICE350N simulator.**

Bit 7 ~ Bit 5: [EM78P350N]: Unimplemented, read as '0'.

Bit 4 (LVDIF) (only for EM78P350N) : **Low voltage Detector interrupt flag.**

LVDEN <RE,3>	LVD1,LVD0 <RE,1,0>	LVD Voltage Interrupt Level	LVDIF
1	11	2.2V	1*
1	10	3.3V	1*
1	01	4.0V	1*
1	00	4.5V	1*
0	XX	NA	0

* If Vdd has crossover at LVD voltage interrupt level as Vdd changes, LVDIF =1.

[With Simulator (C3~C0)]: are IRC calibration bits in IRC oscillator mode. In IRC oscillator mode of ICE350N simulator, these are the IRC calibration bits of IRC oscillator mode.

C3	C2	C1	C0	Frequency (MHz)
0	0	0	0	(1-36%) x F
0	0	0	1	(1-31.5%) x F
0	0	1	0	(1-27%) x F
0	0	1	1	(1-22.5%) x F
0	1	0	0	(1-18%) x F
0	1	0	1	(1-13.5%) x F
0	1	1	0	(1-9%) x F
0	1	1	1	(1-4.5%) x F
1	1	1	1	F (default)
1	1	1	0	(1+4.5%) x F
1	1	0	1	(1+9%) x F
1	1	0	0	(1+135%) x F
1	0	1	1	(1+18%) x F
1	0	1	0	(1+22.5%) x F
1	0	0	1	(1+27%) x F
1	0	0	0	(1+31.5%) x F

Note: 1. Frequency values shown are theoretical and taken from an instance of a high frequency mode. Hence, they are shown for reference only. Definite values depend on the actual process.

2. Similar way of calculation is also applicable for low frequency mode.

Bit 3 (ADWE): ADC wake-up enable bit

0 = Disable ADC wake-up

1 = Enable ADC wake-up

When the ADC Complete is used to enter an interrupt vector or to wake-up the EM78P350N from sleep with AD conversion running, the ADWE bit must be set to "Enable".

Bit 2 (CMPWE): Comparator wake-up enable bit

0 = Disable Comparator wake-up

1 = Enable Comparator wake-up

When the Comparator output status change is used to enter an interrupt vector or to wake-up EM78P350N from sleep, the CMPWE bit must be set to "Enable".

Bit 1 (ICWE): Port 6 input change to wake-up status enable bit

0 = Disable Port 6 input change to wake-up status

1 = Enable Port 6 input change wake-up status

When the Port 6 Input Status Change is used to enter an interrupt vector or to wake-up the EM78P350N from sleep, the ICWE bit must be set to "Enable".

Bit 0 (PWMWE): PWM/Timer wake-up enable bit.

0 = Disable PWM/Timer wake-up

1 = Enable PWM/Timer wake up wake-up

When the PWM/Timer output status change is used to enter an interrupt vector or to wake-up the EM78P350N from sleep, the PWMWE must be set to "Enable", this is reset by software.

6.1.13 RF (Interrupt Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM3IF	PWM2IF	PWM1IF	ADIF	EXIF1	EXIF0	ICIF	TCIF

NOTE

- *"1" means interrupt request; "0" means no interrupt occurs.*
- *RF can be cleared by instruction but cannot be set.*
- *IOCF is the interrupt mask register.*
- *Reading RF will result to "logic AND" of RF and IOCF.*

Bit 7 (PWM3IF): PWM3 (Pulse Width Modulation) interrupt flag. Set when a selected duration is reached. Reset by software.

Bit 6 (PWM2IF): PWM2 (Pulse Width Modulation) interrupt flag. Set when a selected duration is reached. Reset by software.

Bit 5 (PWM1IF): PWM1 (Pulse Width Modulation) interrupt flag. Set when a selected duration is reached. Reset by software.

Bit 4 (ADIF): Interrupt flag for analog to digital conversion. Set when AD conversion is completed. Reset by software.

Bit 3 (EXIF1): External interrupt flag. Set by a falling edge on the /INT1 pin. Reset by software.

Bit 2 (EXIF0): External interrupt flag. Set by a falling edge on the /INT0 pin. Reset by software.

Bit 1 (ICIF): Port 6 input status change interrupt flag. Set when Port 6 input changes. Reset by software.

Bit 0 (TCIF): TCC overflow interrupt flag. Set when TCC overflows. Reset by software.

6.1.14 R10 ~ R3F

All of these are 8-bit general-purpose registers.

6.1.15 Bank 1 R5 (PWM Control Register #1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM3E	PWM2E	PWM1E	"0"	T1EN	T1P2	T1P1	T1P0

Bit 7 (PWM3E): PWM3 enable bit

0 = PWM3 is off (default value), and its related pin carries out the P72 function

1 = PWM3 is on, and its related pin is automatically set as output

Bit 6 (PWM2E): PWM2 enable bit

0 = PWM2 is off (default value), and its related pin carries out the P71 function

1 = PWM2 is on, and its related pin is automatically set as output

Bit 5 (PWM1E): PWM1 enable bit

0 = PWM1 is off (default value), and its related pin carries out the P70 function

1 = PWM1 is on, and its related pin is automatically set to output

Bit 4: Unimplemented, read as '0'

Bit 3 (T1EN): TMR1 enable bit

0 = TMR1 is off (default value)

1 = TMR1 is on

Bit 2 ~ Bit 0 (T1P2 ~ T1P0): TMR1 clock prescale option bits

T1P2	T1P1	T1P0	Prescale
0	0	0	1:2 (default)
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

6.1.16 Bank 1 R6 (PWM Control Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T2EN	T2P2	T2P1	T2P0	T3EN	T3P2	T3P1	T3P0

Bit 7 (T2EN): TMR2 enable bit

0 = TMR2 is off (default value)

1 = TMR2 is on

Bit 6 ~ Bit 4 (T2P2 ~ T2P0): TMR2 clock prescale option bits

T2P2	T2P1	T2P0	Prescale
0	0	0	1:2 (default)
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

Bit 3 (T3EN): TMR3 enable bit

0 = TMR3 is off (default value)

1 = TMR3 is on

Bit 2 ~ Bit 0 (T3P2 ~ T3P0): TMR3 clock prescale option bits

T3P2	T3P1	T3P0	Prescale
0	0	0	1:2 (default)
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

6.1.17 Bank1 R7 (PWM Timer/Counter Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
"0"	"0"	"0"	"0"	T2TS	T2TE	T1TS	T1TE

Bits 7~4: Unimplemented, read as '0'

Bit 3 (T2TS): Timer 2 / Counter 2 signal source

0 = internal instruction cycle clock. If P77 is used as I/O pin, T2TS must be 0

1 = transition on the CNTR2 pin

Bit 2 (T2TE): Timer 2 / Counter 2 signal edge

0 = increment if a transition from low to high takes place on the CNTR2 pin

1 = increment if a transition from high to low takes place on the CNTR2 pin

Bit 1 (T1TS): Timer 1 / Counter 1 signal source

0 = internal instruction cycle clock. If P76 is used as I/O pin, T1TS must be 0

1 = transition on the CNTR1 pin

Bit 0 (T1TE): Timer 1 / Counter 1 signal edge

0 = increment if a transition from low to high takes place on the CNTR1 pin

1 = increment if a transition from high to low takes place on the CNTR1 pin

6.1.18 Bank1 R8 (PRD1H: Most Significant Byte (Bit 9 ~ Bit 2) of PWM1 Time Period)

The content of Bank 1 R8 is the time period (time base) of PWM1. The frequency of PWM1 is the reverse of the period.

6.1.19 Bank1 R9 (PRD2H: Most Significant Byte (Bit 9 ~ Bit 2) of PWM2 Time Period)

The content of Bank 1 R9 is the time period (time base) of PWM2. The frequency of PWM2 is the reverse of the period.

6.1.20 Bank1 RA (PRD3H: Most Significant Byte (Bit 9 ~ Bit 2) of PWM3 Time Period)

The content of Bank 1 RA is the time period (time base) of PWM3. The frequency of PWM3 is the reverse of the period.

6.1.21 Bank1 RB (PRDL: Least Significant Bits of PWM Period Cycle)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
"0"	"0"	PRD3[1]	PRD3[0]	PRD2[1]	PRD2[0]	PRD1[1]	PRD1[0]

Bit 7 & Bit 6: Unimplemented, read as '0'.

Bit 5 & Bit 4 (PRD3[1], PRD3[0]): Least Significant Bits of PWM3 Period Cycle.

Bit 3 & Bit 2 (PRD2[1], PRD2[0]): Least Significant Bits of PWM2 Period Cycle.

Sectioning actions refer to the Reset description. The following actions refer to the section status operation.

Bit 1 & Bit 0 (PRD1[1], PRD1[0]): Least Significant Bits of PWM1 Period Cycle.

6.1.22 Bank 1 RC (DT1H: Most Significant Byte (Bit 9 ~ Bit 2) of PWM1 Duty Cycle)

A specified value keeps the output of PWM1 to remain high until the value matches with TMR1.

6.1.23 Bank 1 RD (DT2H: Most Significant Byte (Bit 9 ~ Bit 2) of PWM2 Duty Cycle)

A specified value keeps the output of PWM2 to remain high until the value matches with TMR2.

6.1.24 Bank1 RE (DT3H: Most Significant Byte (Bit 9 ~ Bit 2) of PWM3 Duty Cycle)

A specified value keeps the output of PWM3 to remain high until the value matches with TMR3.

6.1.25 Bank1 RF (DTL: Least Significant Bits of PWM Duty Cycle)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
"0"	"0"	PWM3[1]	PWM3[0]	PWM2[1]	PWM2[0]	PWM1[1]	PWM1[0]

Bit 7 & Bit 6: Unimplemented, read as '0'

Bit 5 & Bit 4 (PWM3[1], PWM3[0]): Least Significant Bits of PWM3 Duty Cycle

Bit 3 & Bit 2 (PWM2[1], PWM2[0]): Least Significant Bits of PWM2 Duty Cycle

Bit 1 & Bit 0 (PWM1[1], PWM1[0]): Least Significant Bits of PWM1 Duty Cycle

6.1.26 Bank 2 R6 (BOCON: Buzzer Output Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TEN	TCK1	TCK0	FSCS	"0"	"0"	"0"	"0"

Bit 4 (FSCS): High or low frequency select in Function operating

0 = High

1 = Low

Bit 5~Bit 6 (TCK0~TCK1): Keytone output clock source select

TCK1	TCK0	Clock source			Keytone Output Frequency	
		Normal		Slow, Idle	Fc=8M	Fs=32.768K
		FSCS=0	FSCS=1			
0	0	$Fc/(2^{13})$	$Fs/(2^{5})$	$Fs/(2^{5})$	0.976kHz	1.024kHz
0	1	$Fc/(2^{12})$	$Fs/(2^{4})$	$Fs/(2^{4})$	1.953kHz	2.048kHz
1	0	$Fc/(2^{11})$	$Fs/(2^{3})$	$Fs/(2^{3})$	3.906kHz	4.096kHz
1	1	$Fc/(2^{10})$	$Fs/(2^{2})$	$Fs/(2^{2})$	7.812kHz	8.192kHz

Bit 7 (TEN): Key_tone enable control.

0 = Disable

1 = Enable

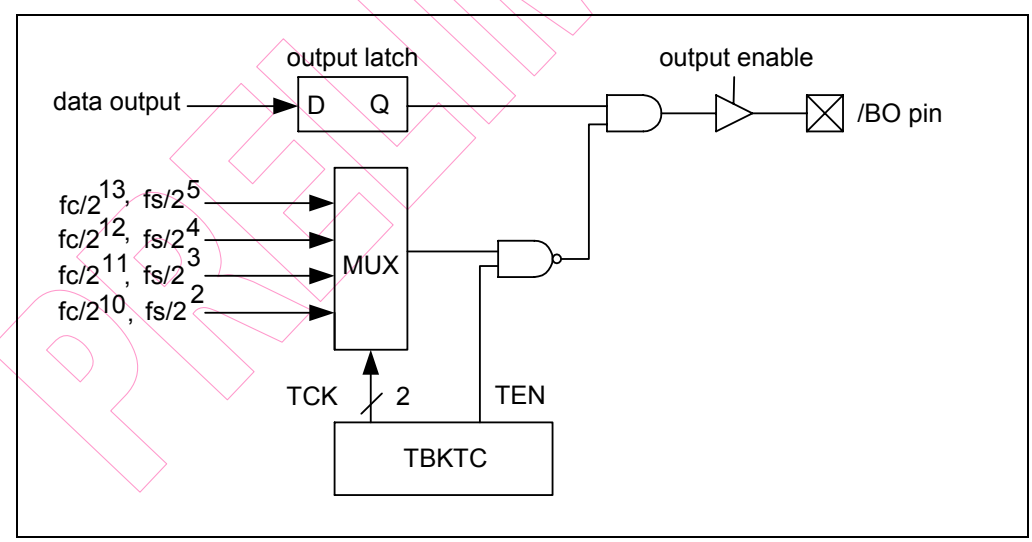


Fig. 6-2 Buzzer Output Pin Configuration

Key tone output can generate 50% duty pulse for driving a piezo-electric buzzer. The P83 must be set to "1" before the keytone is enabled, it can be halted by setting P83 to "0".

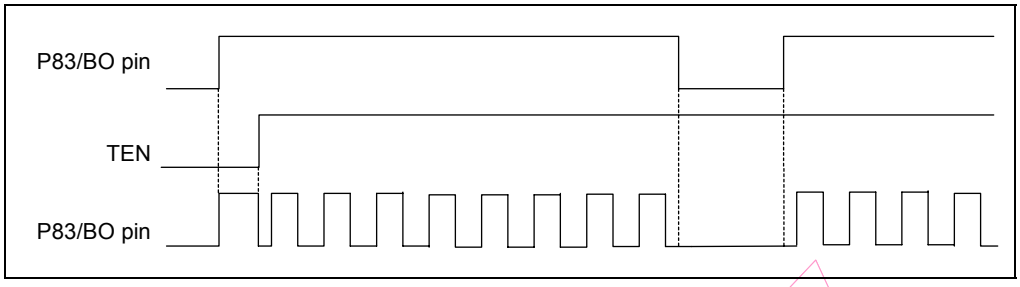


Fig.6-3 Tone Output Pin Timing Chart

Bit 3 ~ Bit 0: Unimplemented, read as '0'

6.1.27 Bank 2 R7 (System Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T1S	T2S	T3S	"0"	"0"	"0"	"0"	IDLE

Bit 7: Timer 1 Clock source

0 = Timer 1 source is used as Main Clock

1 = Timer 1 source is used as Sub clock

Bit 6: Timer 2 Clock Source

0 = Timer 2 source is used as Main Clock

1 = Timer 2 source is used as Sub clock

Bit 5: Timer 3 Clock Source

0 = Timer 3 source is used as Main Clock

1 = Timer 3 source is used as Sub clock

Bit 4 ~ Bit 1: Unimplemented, read as '0'

Bit 0 (IDLE): select idle mode or sleep mode

IDLE = "0" + SLEP Instruction: sub-oscillator (Fs), Fs = 32.768kHz (idle mode). In idle mode, only the sub-oscillator acting as Timer 1, 2, 3 sources, and CPU is halted.

IDLE = "1"+SLEP Instruction: all oscillation stop (sleep mode). In this mode, main-oscillator (Fm) and Fs is not work simultaneously.

IDLE = "0" + SLEP Instruction → idle mode

IDLE = "1" + SLEP Instruction → sleep mode

NOP Instruction must be added after Sleep instruction.

Example: Idle mode: IDLE bit = “0” + SLEP instruction + NOP instruction

Sleep mode: IDLE bit = ”1” + SLEP instruction + NOP instruction.

Only the normal can entering sleep mode, idle mode can’t entering the sleep mode.

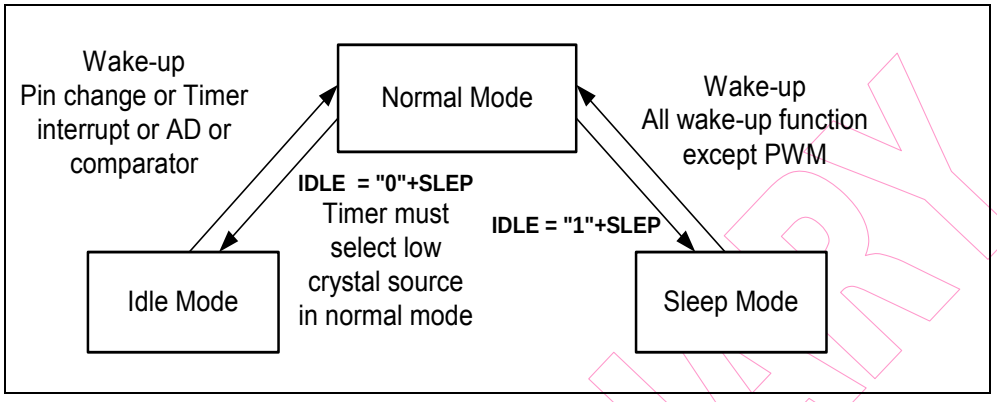


Fig 6-4 CPU Operation Mode

In Sleep mode, the internal oscillator is turned off and all system operation is halted. Sleep mode is released by /Sleep pin (level sensitive or edge sensitive). After warm-up period, the next instruction will be executed which is after the Sleep mode start instruction. Sleep mode can also be released by setting the /Reset pin to low and executing a reset operation.

In Idle mode, only the low crystal source existence, the others crystal source were off. Only the Timer (TCC, Timer 1, Timer 2, Timer 3, PWM1, PWM2, PWM3) can work normally when its clock source select low crystal (if clock source select High crystal, timer will not work). If timer set the PWMWE as “1”, when the timer or PWM occurs interrupt will wake up the CPU and entering normal mode. The TCC overflow will not wake up CPU.

6.1.28 Bank 2 R8 (AISR: ADC Input Select Register)

The AISR register defines the pins of Port 6 as analog inputs or as digital I/O, individually.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADE7	ADE6	ADE5	ADE4	ADE3	ADE2	ADE1	ADE0

Bit 7 (ADE7): AD converter enable bit of P67 pin

0 = Disable AIN7, P67 functions as I/O pin

1 = Enable AIN7, to function as analog input pin

Bit 6 (ADE6): AD converter enable bit of P66 pin

0 = Disable AIN6, P66 functions as I/O pin

1 = Enable AIN6, to function as analog input pin

Bit 5 (ADE5): AD converter enable bit of P65 pin

0 = Disable AIN5, P65 functions as I/O pin

1 = Enable AIN5, to function as analog input pin

Bit 4 (ADE4): AD converter enable bit of P64 pin

0 = Disable AIN4, P64 functions as I/O pin

1 = Enable AIN4 to function as analog input pin

Bit 3 (ADE3): AD converter enable bit of P63 pin

0 = Disable AIN3, P63 functions as I/O pin

1 = Enable AIN3, to function as analog input pin

Bit 2 (ADE2): AD converter enable bit of P62 pin

0 = Disable AIN2, P62 functions as I/O pin

1 = Enable AIN2, to function as analog input pin

Bit 1 (ADE1): AD converter enable bit of P61 pin

0 = Disable AIN1, P61 functions as I/O pin

1 = Enable AIN1, to function as analog input pin

Bit 0 (ADE0): AD converter enable bit of P60 pin.

0 = Disable AIN0, P60 functions as I/O pin

1 = Enable AIN0, to function as analog input pin

NOTE

The P60/AIN0 pin priority is as follows:

P60/ADE0 Priority	
High	Low
AIN0	P60

6.1.29 Bank 2 R9 (ADCON: ADC Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VREFS	CKR1	CKR0	ADRUN	ADPD	ADIS2	ADIS1	ADIS0

Bit 7 (VREFS): The input source of the Vref of the ADC

0 = The Vref of the ADC is connected to Vdd (default value), and the P84/VREF pin carries out the function of P84

1 = The Vref of the ADC is connected to P84/VREF

NOTE

The P84/VREF pin priority is as follows:

P84/VREF Pin Priority	
High	Low
VREF	P84

Bit 6 & Bit 5 (CKR1 & CKR0): The prescaler of ADC oscillator clock rate

00 = 1**:** 16 (default value)

01 = 1**:** 4

10 = 1**:** 64

11 = 1**:** WDT ring oscillator frequency

CKR1:CKR0	Operation Mode	Max. Operation Frequency
00	Fosc/16	4 MHz
01	Fosc/4	1 MHz
10	Fosc/64	16MHz
11	Internal RC	-

Bit 4 (ADRUN): ADC starts to RUN.

0 = Reset upon completion of the conversion. This bit **cannot** be reset through software

1 = an AD conversion is started. This bit can be set by software

Bit 3 (ADPD): ADC Power-down mode

0 = Switch off the resistor reference to save power even while the CPU is operating

1 = ADC is operating

Bit 2 ~ Bit 0 (ADIS2 ~ADIS0): Analog Input Select

000 = AIN0/P60

001 = AIN1/P61

010 = AIN2/P62

011 = AIN3/P63

100 = AIN4/P64

101 = AIN5/P65

110 = AIN6/P66

111 = AIN7/P67

These bits can only be changed when the ADIF bit (see Section 6.1.14) and the ADRUN bit are both LOW.

6.1.30 Bank 2 RA (ADOC: ADC Offset Calibration Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CALI	SIGN	VOF[2]	VOF[1]	VOF[0]	“0”	“0”	“0”

Bit 7 (CALI): Calibration enable bit for ADC offset

0 = Disable Calibration

1 = Enable Calibration

Bit 6 (SIGN): Polarity bit of offset voltage

0 = Negative voltage

1 = Positive voltage

Bit 5 ~ Bit 3 (VOF [2] ~ VOF [0]): Offset voltage bits

VOF[2]	VOF[1]	VOF[0]	EM78P350N
0	0	0	0LSB
0	0	1	2LSB
0	1	0	4LSB
0	1	1	6LSB
1	0	0	8LSB
1	0	1	10LSB
1	1	0	12LSB
1	1	1	14LSB

Bit 2 ~ Bit 0: Unimplemented, read as '0'

6.1.31 Bank 2 RB (ADDATA: Converted Value of ADC)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AD11	AD10	AD9	AD8	AD7	AD6	AD5	AD4

When the AD conversion is completed, the result is loaded into the ADDATA. The ADRUN bit is cleared, and the ADIF (see Section 6.1.14) is set.

RB is read only.

6.1.32 Bank 2 RC (ADDATA1H: Converted Value of ADC)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
"0"	"0"	"0"	"0"	AD11	AD10	AD9	AD8

When the AD conversion is completed, the result is loaded into the ADDATA1H. The ADRUN bit is cleared, and the ADIF (see Section 6.1.14) is set.

RC is read only.

6.1.33 Bank 2 RD (ADDATA1L: Converted Value of ADC)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0

When the AD conversion is completed, the result is loaded into the ADDATA1L. The ADRUN bit is cleared, and the ADIF (see Section 6.1.14) is set.

RD is read only

6.1.34 Bank 2 RE (LVDC: LVD Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
"0"	"0"	"0"	"0"	LVDEN	/LVD	LVD1	LVD0

There is no LVD function in the ICE350N simulator.

Bits 7 ~ 4: Not used, set to "0" at all time.

Bit 3 (LVDEN): Low Voltage Detect Register

0 : disable LVD

1 : enable LVD

Bit 2 (/LVD): Low Voltage Detector. This is a read only bit. When the Vdd pin voltage is lower than the LVD voltage interrupt level (selected by LVD1 and LVD0), this bit will be cleared.

0 : If Vdd < .LVD voltage interrupt level

1 : If Vdd > LVD voltage interrupt level

Bits 1 ~ 0 (LVD1 ~ LVD0) : Low Voltage Detect level select bits

LVDEN <RE,3>	LVD1, LVD0 <RE,1,0>	LVD Voltage Interrupt Level	LVDIF
1	11	2.2V	1*
1	10	3.3V	1*
1	01	4.0V	1*
1	00	4.5V	1*
0	XX	NA	0

*If Vdd has crossover at LVD voltage interrupt level as Vdd changes, LVDIF =1.

6.1.35 Bank 2 RF (TMR3H: Most Significant Bits (Bit 9 ~ Bit 2) of PWM3 Timer)

The contents of RF are read-only.

6.1.36 Bank3 R5 (Pull-low Control Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/PL57	/PL56	/PL55	/PL54	/PL53	/PL52	/PL51	/PL50

Bank 3 R5 register is both readable and writable.

Bit 7 (/PL57): Control bit is used to enable the pull-high of the P57 pin.

0 = Enable pull-low output

1 = Disable pull-low output

Bit 6 (/PL56): Control bit is used to enable the pull-low function of the P56 output pin.

Bit 5 (/PL55): Control bit is used to enable the pull-low function of the P55 output pin.

Bit 4 (/PL54): Control bit is used to enable the pull-low function of the P54 output pin.

Bit 3 (/PL53): Control bit is used to enable the pull-low function of the P53 output pin.

Bit 2 (/PL52): Control bit is used to enable the pull-low function of the P52 output pin.

Bit 1 (/PL51): Control bit is used to enable the pull-low function of the P51 output pin.

Bit 0 (/PL50): Control bit is used to enable the pull-low function of the P50 output pin.

6.1.37 Bank 3 R6 (Pull-Low Control Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/PL67	/PL66	/PL65	/PL64	/PL63	/PL62	/PL61	/PL60

Bank 3 R6 register is both readable and writable.

Bit 7 (/PL67): Control bit is used to enable the pull-high of the P67 pin.

0 = Enable pull-low output

1 = Disable pull-low output

Bit 6 (/PL66): Control bit used to enable the pull-low function of the P66 output pin.

Bit 5 (/PL65): Control bit used to enable the pull-low function of the P65 output pin.

Bit 4 (/PL64): Control bit used to enable the pull-low function of the P64 output pin.

Bit 3 (/PL63): Control bit used to enable the pull-low function of the P63 output pin.

Bit 2 (/PL62): Control bit used to enable the pull-low function of the P62 output pin.

Bit 1 (/PL61): Control bit used to enable the pull-low of function the P61 output pin.

Bit 0 (/PL60): Control bit used to enable the pull-low of function the P60 output pin.

6.1.38 Bank3 R7 (Pull-Low Control Register 3)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/PL77	/PL76	/PL75	/PL74	/PL73	/PL72	/PL71	/PL70

Bank 3 R7 register is both readable and writable.

Bit 7 (/PL77): Control bit is used to enable the pull-high of the P77 pin.

0 = Enable pull-low output

1 = Disable pull-low output

Bit 6 (/PL76): Control bit used to enable the pull-low function of the P76 output pin.

Bit 5 (/PL75): Control bit used to enable the pull-low function of the P75 output pin.

Bit 4 (/PL74): Control bit used to enable the pull-low function of the P74 output pin.

Bit 3 (/PL73): Control bit used to enable the pull-low function of the P73 output pin.

Bit 2 (/PL72): Control bit used to enable the pull-low function of the P72 output pin.

Bit 1 (/PL71): Control bit used to enable the pull-low function of the P71 output pin.

Bit 0 (/PL70): Control bit used to enable the pull-low function of the P70 output pin.

6.1.39 Bank3 R8 (Pull-low Control Register 4)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
"0"	"0"	"0"	/PL84	/PL83	/PL82	/PL81	/PL80

Bank 3 R8 register is both readable and writable.

Bits 7 ~ 5: Not used, set "0" at all time.

Bit 4 (/PL84): Control bit used to enable the pull-high function of the P84 output pin.

0 = Enable pull-low output

1 = Disable pull-low output

Bit 3 (/PL83): Control bit used to enable the pull-low function of the P83 output pin.

Bit 2 (/PL82): Control bit used to enable the pull-low function of the P82 output pin.

Bit 1 (/PL81): Control bit used to enable the pull-low function of the P81 output pin.

Bit 0 (/PL80): Control bit used to enable the pull-low function of the P80 output pin.

6.1.40 Bank3 R9 (Pull-High Control Register 1)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/PH57	/PH56	/PH55	/PH54	/PH53	/PH52	/PH51	/PH50

Bank 3 R9 register is both readable and writable.

Bit 7 (/PH57): Control bit used to enable the pull-high function of the P57 output pin.

0 = Enable pull-high output

1 = Disable pull-high output

Bit 6 (/PH56): Control bit used to enable the pull-high function of the P56 output pin.

Bit 5 (/PH55): Control bit used to enable the pull-high function of the P55 output pin.

Bit 4 (/PH54): Control bit used to enable the pull-high function of the P54 output pin.

Bit 3 (/PH53): Control bit used to enable the pull-high function of the P53 output pin.

Bit 2 (/PH52): Control bit used to enable the pull-high function of the P52 output pin.

Bit 1 (/PH51): Control bit used to enable the pull-high function of the P51 output pin.

Bit 0 (/PH50): Control bit used to enable the pull-high function of the P50 output pin.

6.1.41 Bank 3 RA (Pull-High Control Register 2)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/PH67	/PH66	/PH65	/PH64	/PH63	/PH62	/PH61	/PH60

Bank 3 RA register is both readable and writable.

Bit 7 (/PH67): Control bit is used to enable the pull-high of the P67 pin.

0 = Enable pull-high output

1 = Disable pull-high output

Bit 6 (/PH66): Control bit used to enable the pull-high function of the P66 output pin.

Bit 5 (/PH65): Control bit used to enable the pull-high function of the P65 output pin.

Bit 4 (/PH64): Control bit used to enable the pull-high function of the P64 output pin.

Bit 3 (/PH63): Control bit used to enable the pull-high function of the P63 output pin.

Bit 2 (/PH62): Control bit used to enable the pull-high function of the P62 output pin.

Bit 1 (/PH61): Control bit used to enable the pull-high function of the P61 output pin.

Bit 0 (/PH60): Control bit used to enable the pull-high function of the P60 output pin.

6.1.42 Bank 3 RB (Pull-high Control Register 3)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
/PH77	/PH76	/PH75	/PH74	/PH73	/PH72	/PH71	/PH70

Bank 3 RB register is both readable and writable.

Bit 7 (/PH77): Control bit used to enable the pull-high function of the P77 output pin.

0 = Enable pull-high output

1 = Disable pull-high output

Bit 6 (/PH76): Control bit used to enable the pull-high function of the P76 output pin.

Bit 5 (/PH75): Control bit used to enable the pull-high function of the P75 output pin.

Bit 4 (/PH74): Control bit used to enable the pull-high function of the P74 output pin.

Bit 3 (/PH73): Control bit used to enable the pull-high function of the P73 output pin.

Bit 2 (/PH72): Control bit used to enable the pull-high function of the P72 output pin.

Bit 1 (/PH71): Control bit used to enable the pull-high function of the P71 output pin.

Bit 0 (/PH70): Control bit used to enable the pull-high function of the P70 output pin.

6.1.43 Bank 3 RC (Pull-high Control Register 4)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
“0”	“0”	“0”	/PH84	/PH83	/PH82	/PH81	/PH80

Bank 3 RC register is both readable and writable.

Bits 7 ~ 5: Not used, set to “0” at all time.

Bit 4 (/PH84): Control bit is used to enable the pull-high function of the P84 output pin.

0 = Enable pull-low output

1 = Disable pull-low output

Bit 3 (/PH83): Control bit used to enable the pull-high function of the P83 output pin.

Bit 2 (/PH82): Control bit used to enable the pull-low function of the P82 output pin.

Bit 1 (/PH81): Control bit used to enable the pull-low function of the P81 output pin.

Bit 0 (/PH80): Control bit used to enable the pull-low function of the P80 output pin.

6.1.44 Bank 3 RD (TMR1H: Most Significant Bits (Bit9 ~ Bit2) of PWM1 Timer)

The contents of RD are read-only.

6.1.45 Bank 3 RE (TMR2H: Most Significant Bits (Bit 9 ~ Bit 2) of PWM2 Timer)

The contents of RE are read-only.

6.1.46 Bank 3 RF (TMRL: Least Significant Bits of PWM Timer)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
"0"	"0'	TMR3[1]	TMR3[0]	TMR2[1]	TMR2[0]	TMR1[1]	TMR1[0]

The contents of RF are read only,

Bit 7 ~ Bit 6: Unimplemented, read as "0".

Bit 5 ~ Bit 4: (TMR3 [1], TMR3 [0]): Most Significant Bits of PWM3 Timer.

Bit 3 ~ Bit 2: (TMR2 [1], TMR2 [0]): Most Significant Bits of PWM2 Timer.

Bit 1 ~ Bit 0: (TMR1 [1], TMR1 [0]): Most Significant Bits of PWM1 Timer.

6.2 Special Purpose Registers

6.2.1 A (Accumulator)

Internal data transfer operation, or instruction operand holding usually involves the temporary storage function of the Accumulator. The Accumulator is not an addressable register.

6.2.2 CONT (Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTE	INT	TS	TE	PSTE	PST2	PST1	PST0

Bit 7 (INTE): INT signal edge

0 = interrupt occurs at the rising edge on the INT pin

1 = interrupt occurs at the falling edge on the INT pin

Bit 6 (INT): Interrupt enable flag

0 = masked by DISI or hardware interrupt

1 = enabled by the ENI/RETI instructions

This bit is readable only.

Bit 5 (TS): TCC signal source

0 = internal instruction cycle clock. If P56 is used as I/O pin, TS must be 0.

1 = transition on the TCC pin

Bit 4 (TE): TCC signal edge

0 = increment if the transition from low to high takes place on the TCC pin

1 = increment if the transition from high to low takes place on the TCC pin.

Bit 3 (PSTE): Prescaler enable bit for TCC

0 = prescaler disable bit. TCC rate is 1:1

1 = prescaler enable bit. TCC rate is set as Bit 2 ~ Bit 0.

Bit 2 ~ Bit 0 (PST2 ~ PST0): TCC prescaler bits

PST2	PST1	PST0	TCC Rate
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

Note: Tcc time-out period [1/Fosc x prescaler x 256 (Tcc cnt) x 1 (CLK=2)]
Tcc time-out period [1/Fosc x prescaler x 256 (Tcc cnt) x 2 (CLK=4)]

6.2.3 IOC5 ~ IOC8 (I/O Port Control Register)

0 = defines the relative I/O pin as outpu

1 = puts the relative I/O pin into high impedance

IOC5, **IOC6**, **IOC7, and IOC8** registers are all readable and writable.

6.2.4 IOC9 (T4CON: Timer 4 Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SPIE	SPIF	–	TM4IF	“0”	TM4E	TM4P1	TM4P0

Bit 7(SPIIE): SPI Interrupt enable bit

0 = Disable SPI interrupt

1 = Enable SPI interrupt

Bit 6 (SPIIF): SPI interrupt flag. Set by data transmission complete, flag is cleared by software.

Bit 4 (TM4IF) Timer 4 interrupt flag. Set by the comparator during Timer 4 application, flag is cleared by software.

Bit 3: Unimplemented, read as ‘0’

Bit 2 (TM4E): Timer 4 Function Enable bit

0 = Disable Timer 4 function as default

1 = Enable Timer 4 function

Bit 1~Bit 0 (TM4P): Timer4 Prescaler bit

TM4P1	TM4P0	Prescaler Rate
0	0	1:1
0	1	1:4
1	0	1:8
1	1	1:16

6.2.5 IOCA (TCMPCON: Comparator Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
"0"	"0"	"0"	CMPIF	CMPIE	CPOUT	COS1	COS0

Bits 7~ 5: Unimplemented, read as '0'

Bit 4 (CMPIF): Comparator interrupt flag. Set when a change occurs in the output of Comparator. Reset by software.

Bit 3 (CMPIE): CMPIF interrupt enable bit

0 = Disable CMPIF interrupt

1 = Enable CMPIF interrupt

When the Comparator output status change is used to enter interrupt vector or to enter next instruction, the CMPIE bit must be set to "Enable".

Bit 2 (CPOUT): the result of the comparator output

Bit 1 ~ Bit 0 (COS1 ~ COS0): Comparator/OP Select bits

COS1	COS0	Function Description
0	0	The Comparator and OP arenot used. P56 functions as normal I/O pin
0	1	Functions as Comparator and P56 functions as normal I/O pin
1	0	Functions as Comparator and P56 functions as Comparator output pin (CO)
1	1	Functions as OP and P56 functions as OP output pin (CO)

6.2.6 IOCE (WDT Control Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WDTE	EIS0	EIS1	PSWE	PSW2	PSW1	PSW0	LVDIE

Bit 7 (WDTE): Control bit used to enable the Watchdog Timer

0 = Disable WDT

1 = Enable WDT

WDTE is both readable and writable.

Bit 6 (EIS0): Control bit used to define the function of the P52 (/INT0) pin

0 = P52, normal I/O pin

1 = /INT0, external interrupt pin. In this case, the I/O control bit of P52 (Bit 2 of IOC50) must be set to "1", and tied to a pull-high register (75 KΩ)

NOTE

- *When EIS0 is "0," the path of /INT0 is masked. When EIS0 is "1," the status of /INT0 pin can also be read by way of reading Port 5 (R5). Refer to Fig. 6-4 (I/O Port and I/O Control Register Circuit for P52 (/INT0)) under Section 6.4 (I/O Ports).*
- *EIS0 is both readable and writable.*

Bit 5 (EIS1): Control bit used to define the function of the P53 (/INT1) pin

0 = P53, normal I/O pin

1 = /INT1, external interrupt pin. In this case, the I/O control bit of P53 (Bit 3 of IOC50) must be set to "1", and tied to a pull-high register (75 KΩ).

NOTE

- *When EIS1 is "0," the path of /INT1 is masked. When EIS1 is "1," the status of /INT1 pin can also be read by way of reading Port 5 (R5). Refer to Fig. 6-4 (I/O Port and I/O Control Register Circuit for P53 (/INT1)) under Section 6.4 (I/O Ports).*
- *EIS1 is both readable and writable.*

Bit 4 (PSWE): Prescaler enable bit for WDT

0 = prescaler disable bit. WDT rate is 1:1

1 = prescaler enable bit. WDT rate is set as Bit 4~Bit 2

Bit 3 ~ Bit 1 (PSW2 ~ PSW0): WDT prescaler bits.

PSW2	PSW1	PSW0	WDT Rate
0	0	0	1:2
0	0	1	1:4
0	1	0	1:8
0	1	1	1:16
1	0	0	1:32
1	0	1	1:64
1	1	0	1:128
1	1	1	1:256

Bit 0 (LVDIE) LVDIF interrupt enable bit.

0 = disable LVDIF interrupt

1 = enable LVDIF interrupt

6.2.7 IOCF (Interrupt Mask Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM3IE	PWM2IE	PWM1IE	ADIE	EXIE1	EXIE0	ICIE	TCIE

NOTE

- *IOCF register is both readable and writable*
- *Individual interrupt is enabled by setting its associated control bit in the IOCF to "1."*
- *Global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction. Refer to Fig. 6-8 (Interrupt Input Circuit) under Section 6.6 (Interrupt).*

Bit 7 (PWM3IE): PWM3IF interrupt enable bit
0 = Disable PWM3 interrupt
1 = Enable PWM3 interrupt

Bit 6 (PWM2IE): PWM2IF interrupt enable bit
0 = Disable PWM2 interrupt
1 = Enable PWM2 interrupt

Bit 5 (PWM1IE): PWM1IF interrupt enable bit
0 = Disable PWM1 interrupt
1 = Enable PWM1 interrupt

Bit 4 (ADIE): ADIF interrupt enable bit
0 = Disable ADIF interrupt
1 = Enable ADIF interrupt
When the ADC Complete status is used to enter an interrupt vector or to enter next instruction, the ADIE bit must be set to “Enable.“

Bit 3 (EXIE1): EXIF External 1 interrupt enable bit
0 = Disable EXIF interrupt
1 = Enable EXIF interrupt

Bit 2 (EXIE0): EXIF External 0 interrupt enable bit
0 = Disable EXIF interrupt
1 = Enable EXIF interrupt

Bit 1 (ICIE): ICIF interrupt enable bit
0 = Disable ICIF interrupt
1 = Enable ICIF interrupt
If Port 6 Input Status Change Interrupt is used to enter an interrupt vector or to enter next instruction, the ICIE bit must be set to “Enable“.

Bit 0 (TCIE): TCIF interrupt enable bit.
0 = Disable TCIF interrupt
1 = Enable TCIF interrupt

6.3 TCC/WDT and Prescaler

There are two 8-bit counters available as prescalers for the TCC and WDT respectively. The PST0 ~ PST2 bits of the CONT register are used to determine the ratio of the TCC prescaler, and the PWR0 ~ PWR2 bits of the IOCE0 register are used to determine the prescaler of WDT. The prescaler counter is cleared by the instructions each time such instructions are written into TCC. The WDT and prescaler will be cleared by the "WDTC" and "SLEP" instructions. Fig. 6-2 (next page) depicts the block diagram of TCC/WDT.

TCC (R1) is an 8-bit timer/counter. The TCC clock source can be an internal clock or external signal input (edge selectable from the TCC pin). If TCC signal source is from an internal clock, the TCC will be incremented by 1 at every instruction cycle (without prescaler). Referring to Fig. 6-2, CLK=Fosc/2 or CLK=Fosc/4 is dependent to the Code Option bit <CLKS>. CLK=Fosc/2 if the CLKS bit is "0," and CLK=Fosc/4 if the CLKS bit is "1." If the TCC signal source is from an external clock input, TCC will be incremented by 1 at every falling edge or rising edge of the TCC pin. The TCC pin input time length (kept in High or Low level) must be greater than 1CLK.

NOTE

The internal TCC will stop running when sleep mode occurs. However, during AD conversion, when TCC is set to "SLEP" instruction, if the ADWE bit of RE register is enabled, the TCC will keep on running.

The watchdog timer is a free running on-chip RC oscillator. The WDT will keep on running even when the oscillator driver has been turned off (i.e., in sleep mode). During normal operation or sleep mode, a WDT time-out (if enabled) will cause the device to reset. The WDT can be enabled or disabled at any time during normal mode through software programming. Refer to WDTE bit of IOCE0 register (Section 6.2.10 *IOCE0 (WDT Control Register)*. With no prescaler, the WDT time-out duration is approximately 18ms.[1]

[1] VDD=5V, Setup time period = 16.5ms ± 30%.
VDD=3V, Setup time period = 18ms ± 30%.

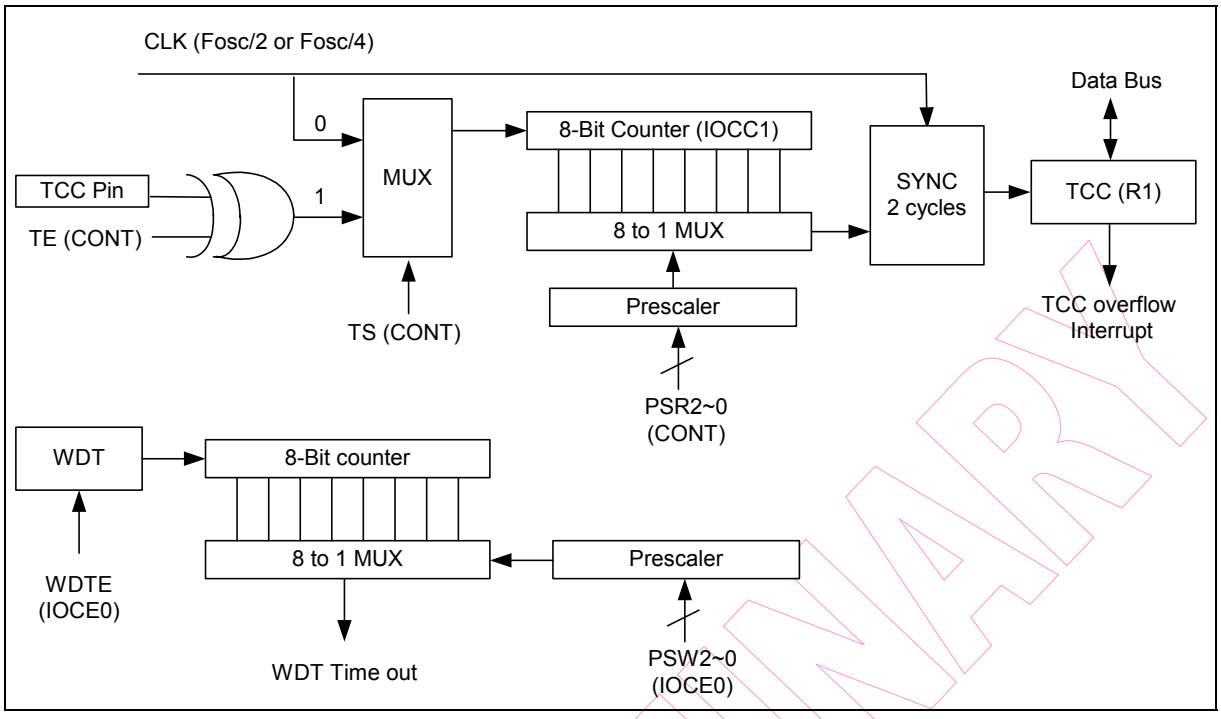
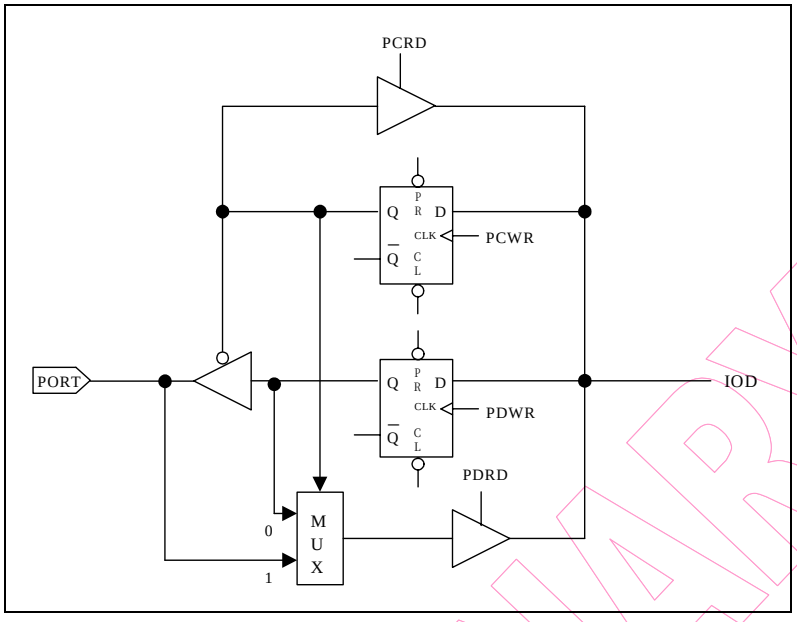


Fig. 6-2 TCC and WDT Block Diagram

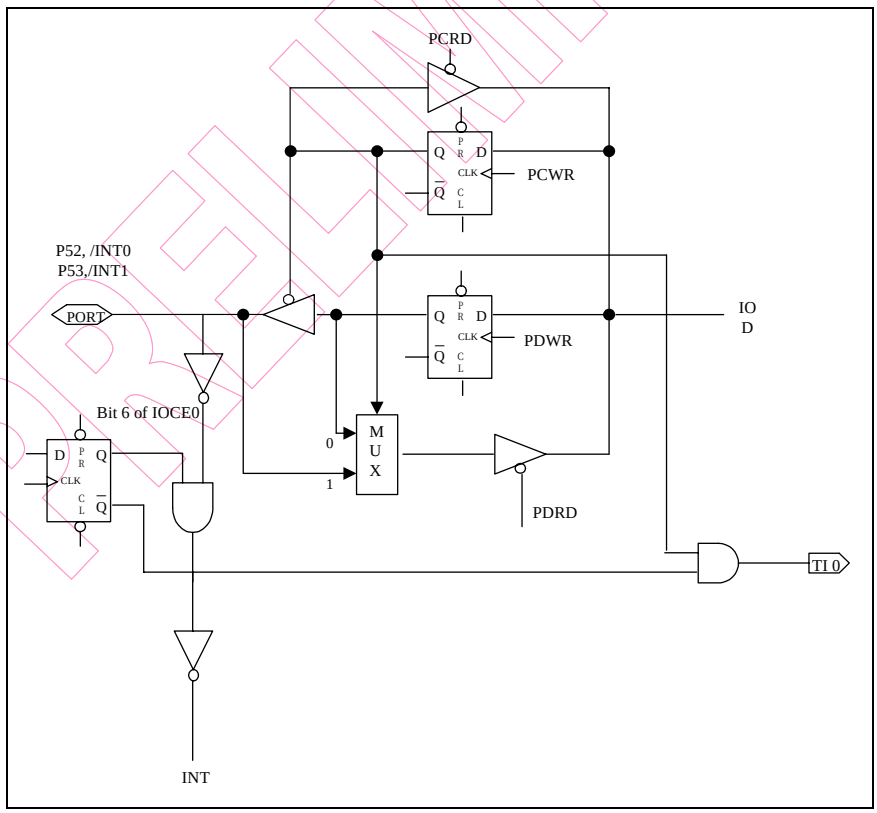
6.4 I/O Ports

The I/O registers (Port 5, Port 6, Port 7 and Port8) are bidirectional tri-state I/O ports. The Pull-high and Pull-down functions can be set internally by IOCB0, IOCC0, and IOCD0 respectively. Port 6 features an input status change interrupt (or wake-up) function. Each I/O pin can be defined as "input" or "output" pin by the I/O control registers (IOC50 ~ IOC80). The I/O registers and I/O control registers are both readable and writable. The I/O interface circuits for Port 5, Port 6, and Port 7 are illustrated in Figures 6-3, 6-4, & 6-5 respectively (see next page). Port 6 with Input Change Interrupt/Wake-up is shown in Fig. 6-6.



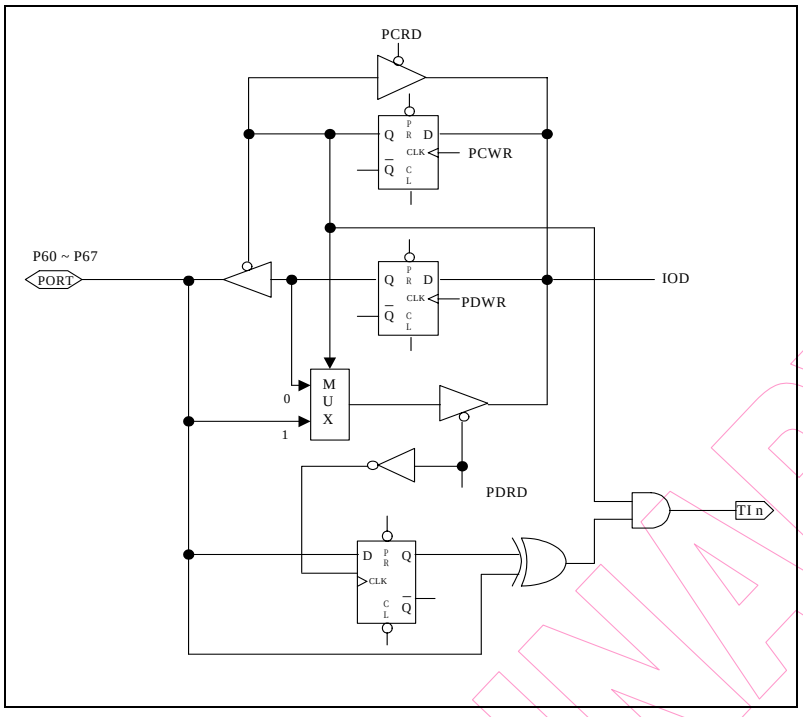
Note: Pull-high and Open-drain are not shown in the figure.

Fig. 6-3 I/O Port and I/O Control Register Circuit for Port 5, Port 7, and Port 8



Note: Pull-high and Open-drain are not shown in the figure.

Fig. 6-4 I/O Port and I/O Control Register Circuit for P52 (/INT0) and P53 (/INT1)



Note: Pull-high (down) and Open-drain are not shown in the figure.

Fig. 6-5 I/O Port and I/O Control Register Circuit for Port 6

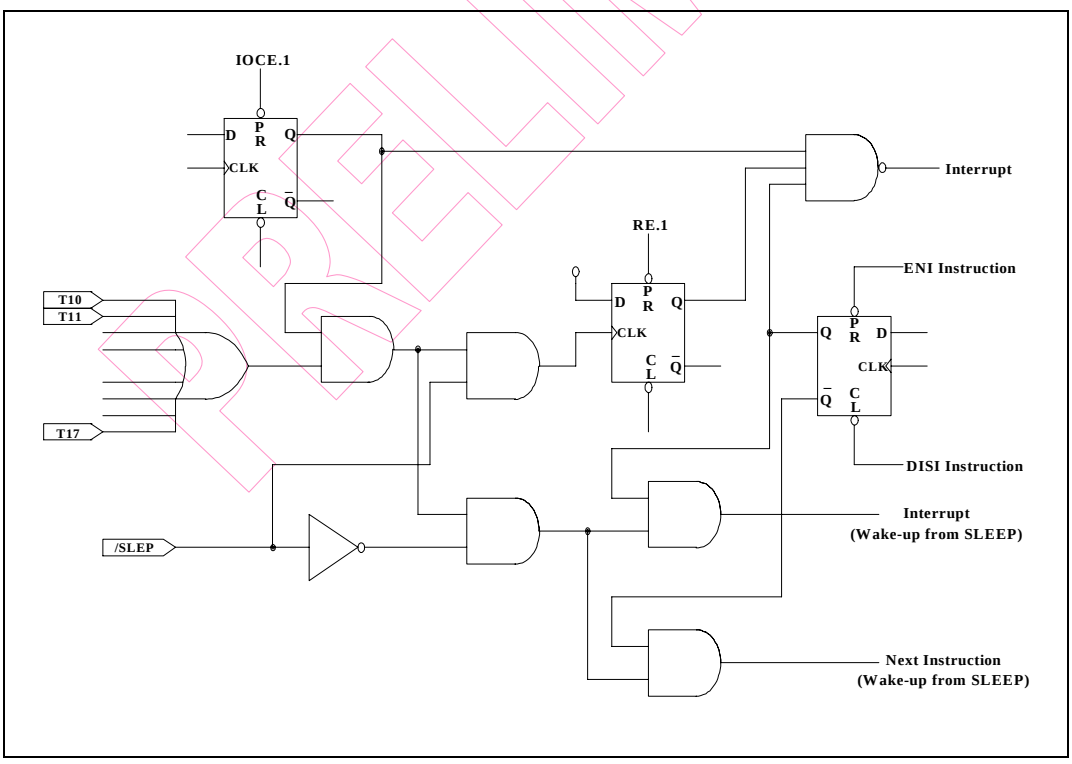


Fig. 6-6 Port 6 Block Diagram with Input Change Interrupt/Wake-up

6.4.1 Usage of Port 6 Input Change Wake-up/Interrupt Function

(1) Wake-up	(2) Wake-up and Interrupt
(a) Before Sleep	(a) Before Sleep
1. Disable WDT	1. Disable WDT
2. Read I/O Port 6 (MOV R6,R6)	2. Read I/O Port 6 (MOV R6,R6)
3. Execute "ENI" or "DISI"	3. Execute "ENI" or "DISI"
4. Enable wake-up bit (Set RE ICWE =1)	4. Enable wake-up bit (Set RE ICWE =1)
5. Execute "SLEP" instruction	5. Enable interrupt (Set IOCF ICIE =1)
(b) After wake-up	6. Execute "SLEP" instruction
→ Next instruction	(b) After wake-up
	1. IF "ENI" → Interrupt vector (008H)
	2. IF "DISI" → Next instruction

(3) Interrupt
(a) Before Port 6 pin change
1. Read I/O Port 6 (MOV R6,R6)
2. Execute "ENI" or "DISI"
3. Enable interrupt (Set IOCF ICIE =1)
(b) After Port 6 pin changed (interrupt)
1. IF "ENI" → Interrupt vector (008H)
2. IF "DISI" → Next instruction

6.5 Serial Peripheral Interface Mode

6.5.1 Overview and Features

Overview:

Figures 6-7, 6-8, and 6-9 shows how the EM78P350N communicates with other devices through SPI module. If the EM78P350N is a master controller, it sends clock through the SCK pin. A couple of 8-bit data are transmitted and received at the same time. However, if EM78P350N is defined as a slave, its SCK pin could be programmed as an input pin. Data will continue to be shifted based on both the clock rate and the selected edge. The SPIS Bit 7 (DORD) can also be set to determine the SPI transmission order, SPIC Bit 3 (SDOC) to control SDO pin after serial data output status and SPIS Bit 6 (TD1), Bit 5 (TD0) determines the SDO status output delay times.

Features:

- Operation in either Master mode or Slave mode
- Three-wire or four-wire full duplex synchronous communication
- Programmable baud rates of communication,
- Programming the clock polarity, (RD Bit 7)
- Interrupt flag available for the read buffer full,

- SPI transmission order
- After serial data output SDO status select
- SDO status output delay times
- SPI handshake pin
- Up to 8 MHz (maximum) bit frequency,

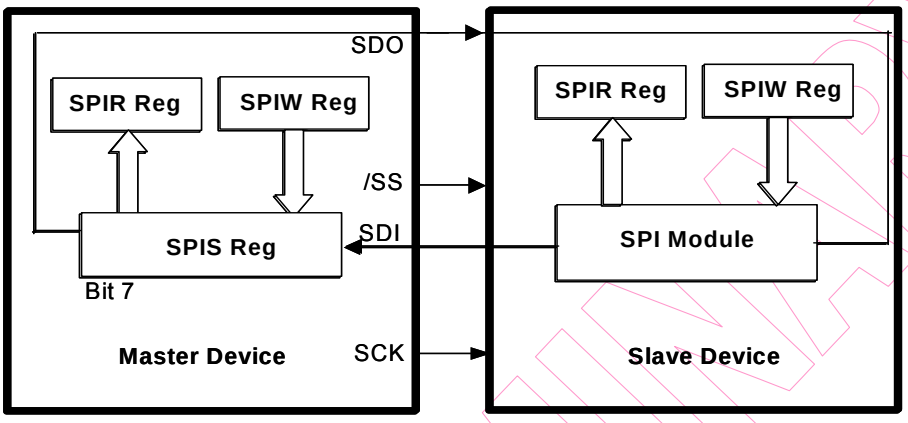


Fig. 6-7 SPI Master/Slave Communication

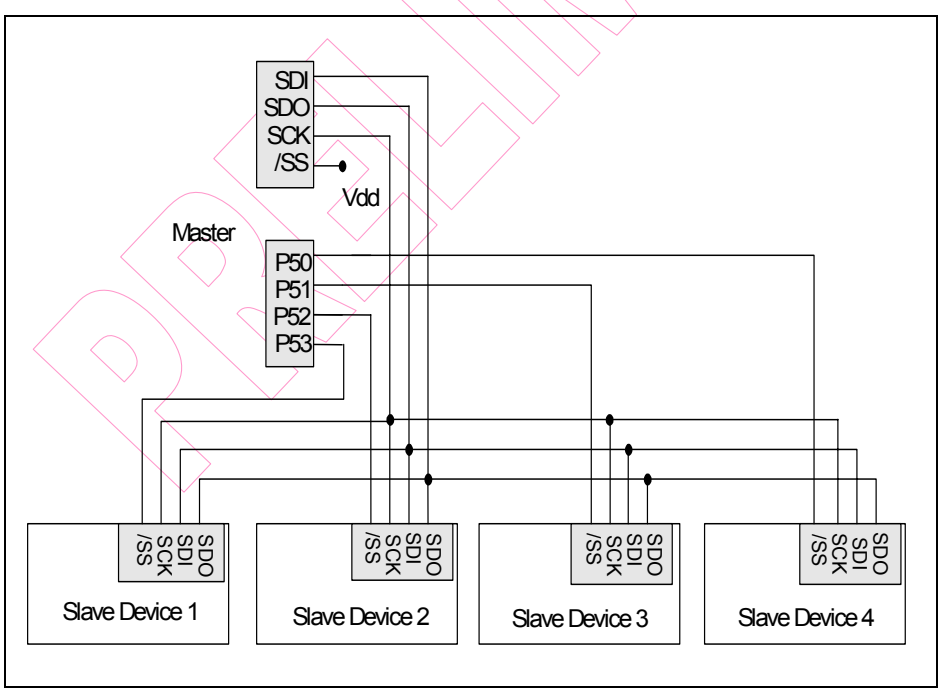


Fig. 6-8 SPI Configuration of Single-Master and Multi-Slave

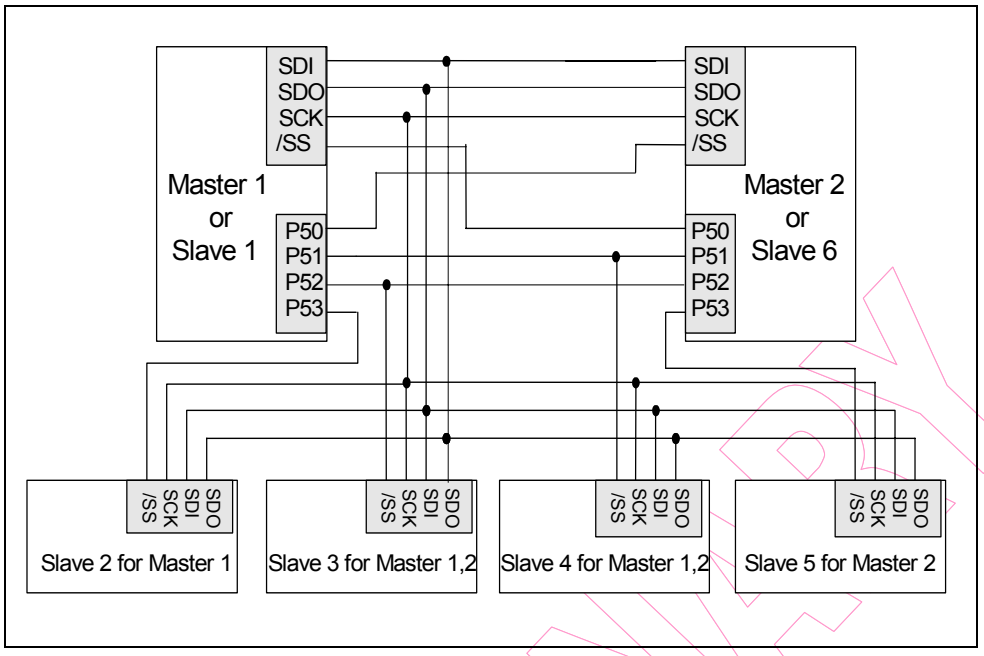


Fig. 6-9 SPI Configuration of Single-Master and Multi-Slave

6.5.2 SPI Function Description

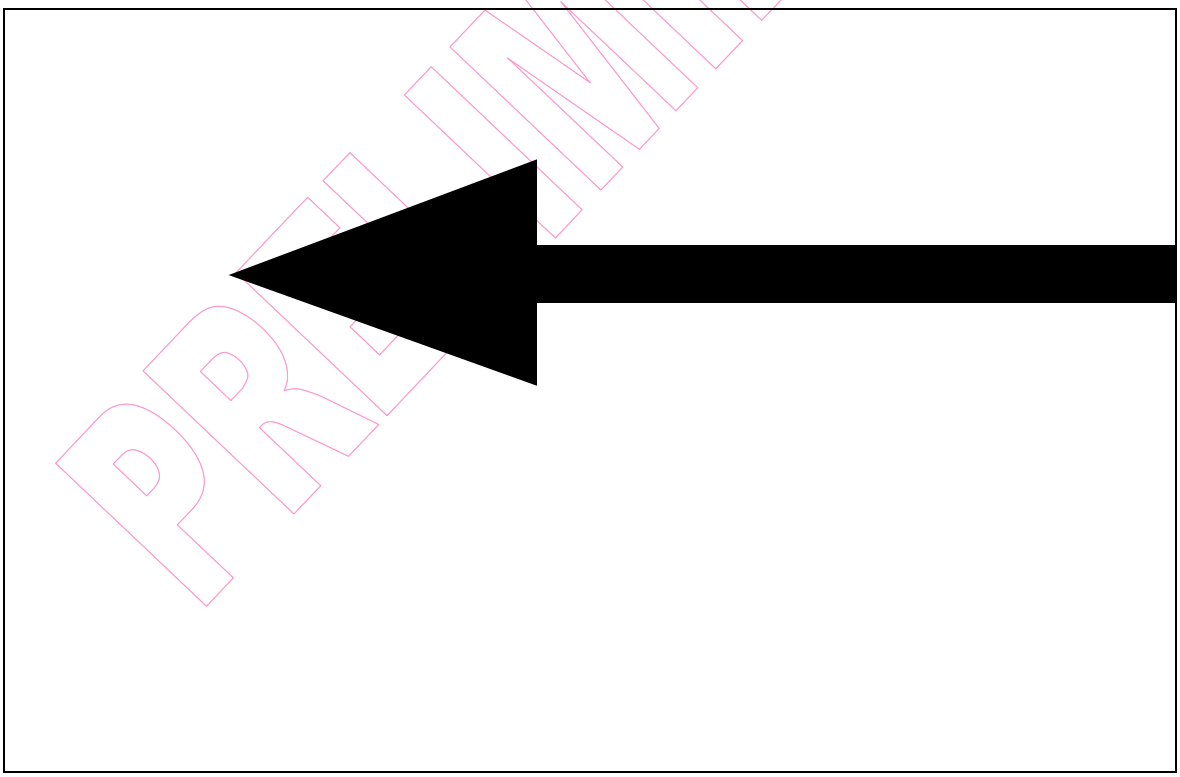


Fig. 6-10 SPI Block Diagram

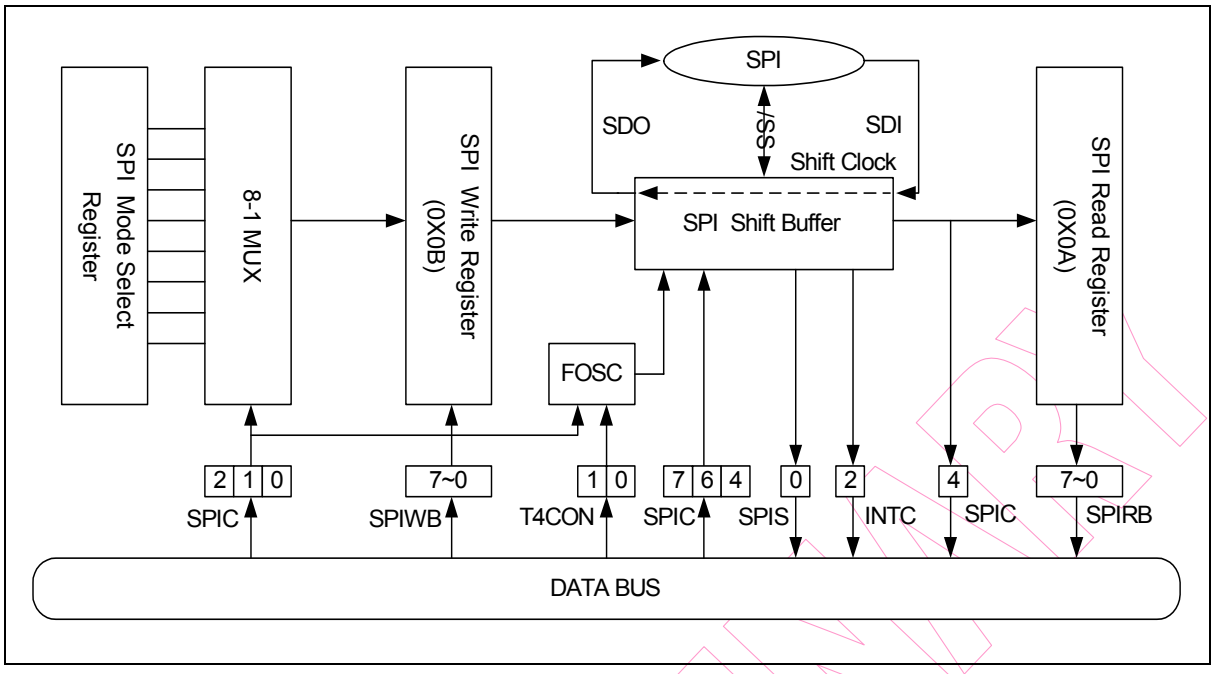


Fig. 6-11 SPI Transmission Function Block Diagram

Below are the functions of each block and explanations on how to carry out the SPI communication with the signals depicted in Fig.6-12 and Fig.6-13:

- P82/Sin: Serial Data In
- P81/Sout: Serial Data Out
- P80/SCK: Serial Clock
- P75//SS: /Slave Select (Option). This pin (/SS) may be required in slave mode.
- RBF: Set by Buffer Full Detector, and read SPIRB to reset.
- Buffer Full Detector: Sets to 1 when an 8-bit shifting is completed.
- SSE: Loads the data in SPIS register, and begin to shift
- SPIS reg.:Shifting byte in and out. The MSB is shifted first. Both the SPIS and the SPIW registers are loaded at the same time. Once data are written, SPIS starts transmission/reception. The data received will be moved to the SPIR register as the shifting of the 8-bit data is completed. The RBF (Read Buffer Full) flag and the SPIF (SPI Interrupt) flag are then set.
- SPIR reg.:Read buffer. The buffer will be updated as the 8-bit shifting is completed. The data must be read before the next reception is completed. The RBF flag is cleared as the SPIR register reads.
- SPIW reg.:Write buffer. The buffer will ignore any attempts to write until the 8-bit shifting is completed.

The SSE bit will be kept in “1“if the communication is still undergoing. This flag must be cleared as the shifting is completed. Users can determine if the next write attempt is available.

- SBRS2~SBRS0: Programming the clock frequency/rates and sources.
- Clock Select: Selecting either the internal or the external clock as the shifting clock.
- Edge Select: Selecting the appropriate clock edges by programming the CES bit

6.5.3 SPI Signal and Pin Description

The detailed functions of the four pins, SDI, SDO, SCK, and /SS, which are shown in Fig. 6-9, are as follows:

Sin/P82:

- Serial Data In
- Receive sequentially, the Most Significant Bit (MSB) first, Least Significant Bit (LSB) last.
- Defined as high-impedance, if not selected.
- Program the same clock rate and clock edge to latch on both the master and slave devices.
- The byte received will update the transmitted byte.
- The RBF bit (located in Register 0x0C) will be set as the SPI operation is completed.
- Timing is shown in Fig.6-12 and 6-13.

Sout/P81:

- Serial Data Out
- Transmit sequentially; the Most Significant Bit (MSB) first, Least Significant Bit (LSB) last.
- Program the same clock rate and clock edge to latch on both the master and slave devices.
- The received byte will update the transmitted byte.
- The CES (located in Register 0x0D) bit will be reset, as the SPI operation is completed.
- Timing is shown in Fig.6-10 and 6-11.

SCK/P80 (Pin 6):

- Serial Clock
- Generated by a master device
- Synchronize the data communication on both the SDI and SDO pins.
- The CES (located in Register 0x0D) is used to select the edge to communicate.
- The SBR0~SBR2 (located in Register 0x0D) is used to determine the baud rate of communication.
- The CES, SBR0, SBR1, and SBR2 bits have no effect in slave mode
- Timing is shown in Fig.6-12 and 6-13.

/SS/P75 (Pin 4):

- Slave Select; negative logic
- Generated by a master device to signify the slave to receive data
- Goes low before the first cycle of SCK appears, and remains low until the last (eighth) cycle is completed,
- Ignores the data on the SDI and SDO pins while /SS is high, since the SDO is no longer driven.
- Timing is shown in Fig.6-12 and 6-13.

6.5.4 Programming the Related Registers

As the SPI mode is defined, the related registers of this operation are shown in Table 2 and Table 3.

Table 1 Related Control Registers of the SPI Mode

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0D	*SPIC/RD	CES	SPIE	SRO	SSE	SOUTC	SBR2	SBR1	SBR0
NA	T4CR/IOC9	SPIIE	SPIF	–	TM4IF	“0”	TM4E	TM4P1	TM4P0

SPIC: SPI Control Register.

Bit 7 (CES): Clock Edge Select bit

0 = Data shifts out on rising edge, and shifts in on falling edge. Data is on hold during the low level.

1 = Data shifts out on falling edge, and shifts in on rising edge. Data is on hold during the high level.

Bit 6 (SPIE): SPI Enable bit

0 = Disable SPI mode

1 = Enable SPI mode

Bit 5 (SRO): SPI Read Overflow bit

0 = No overflow occurs

1 = A new data is received while the previous data is still being on hold in the SPIRB register. Under this condition, the data in SPIS register will be destroyed. To avoid setting this bit, users should read the SPIRB register even if the transmission is implemented only.

NOTE

This can only occur in slave mode.

Bit 4 (SSE): SPI Shift Enable bit

0 = Reset as soon as the shifting is completed and the next byte is ready to shift.

1 = Start to shift, and remains on 1 while the current byte continues to transmit.

NOTE

This bit can be reset by hardware only.

Bits 2~0 (SBRS):SPI Baud Rate Select Bits

SBRS2 (Bit 2)	SBRS1 (Bit 1)	SBRS0 (Bit 0)	Mode	Baud Rate
0	0	0	Master	Fsco/2
0	0	1	Master	Fsco/4
0	1	0	Master	Fsco/8
0	1	1	Master	Fsco/16
1	0	0	Master	Fsco/32
1	0	1	Slave	/SS enable
1	1	0	Slave	/SS disable
1	1	1	Master	TMR4/2

Note: In Master mode, /SS is disabled.

T4CR: Timer 4 Control Register

Bit 7(SPIIE): SPI Interrupt enable bit

0 : Disable SPI interrupt

1 : Enable SPI interrupt

Bit 6 (SPIIF): SPI interrupt flag. Set by data transmission complete, flag by software.

Bit 5 (TM4IE): TM4IE interrupt enable bit

0 : Disable TM4IE interrupt

1 : Enable TM4IE interrupt

Bit 3 (TM4IF): Timer 4 interrupt flag. Set by the comparator at Timer 4 application, flag is cleared by software.

Bit 3: Unimplemented, read as '0'

Bit 2 (TM4E): Timer 4 Function Enable bit

0 : Disable Timer 4 function (default)

1 : Enable Timer 4 function

Bit 1~Bit 0 (TM4P): Timer 4 Prescaler bit

TM4P1	TM4P0	Prescaler Rate
0	0	1:1
0	1	1:4
1	0	1:8
1	1	1:16

Table 2 Related Status/Data Registers of the SPI Mode

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X0A	SPIRB/RA	SRB7	SRB6	SRB5	SRB4	SRB3	SRB2	SRB1	SRB0
0x0B	SPIWB/RB	SWB7	SWB6	SWB5	SWB4	SWB3	SWB2	SWB1	SWB0
0x0C	SPIS/RC	DORD	TD1	TD0	T4ROS	OD3	OD4	-	RBF

SPIRB: SPI Read Buffer. Once the serial data is received completely, it will load to SPIRB from SPISR. The RBF bit in the SPIS register will also be set.

SPIWB: SPI Write Buffer. As a transmitted data is loaded, the SPIS register stands by and start to shift the data when sensing SCK edge with SSE set to "1".

SPIS: SPI Status register

Bit 7 (DORD): Data transmission order

0 : Shift left (MSB first)

1 : Shift right (LSB first)

Bit 6 ~ Bit 5: SDO Status Output Delay Times Options. There is no action in slave mode.

TD1	TD0	Delay Time
0	0	8 CLK
0	1	16 CLK
1	0	24 CLK
1	1	32 CLK

Bit 4 (T4ROS): Timer 4 Read Out Buffer Select Bit

0 : Read Value from Timer 4 Preset Register

1 : Read Value from Timer 4 Counter Register

Bit 3 (OD3) Open-Drain Control bit (P81)

0 : Open-drain disable for Sout

1 : Open-drain enable for Sout

Bit 2 (OD4): Open Drain-Control bit (P80)

0 : Open-drain disable for SCK

1 : Open-drain enable for SCK

Bit 0 (RBF): Read Buffer Full flag

0 : Receive is ongoing, SPIB is empty

1 : Receive is completed, SPIB is full

6.5.5 SPI Mode Timing

The edge of SCK is selected by programming bit CES. The waveform shown in Fig. 6-12 is applicable regardless of whether the EM78P350N is in master or slave mode with /SS disabled. However, the waveform in Fig. 6-13 can only be implemented in slave mode with /SS enabled.

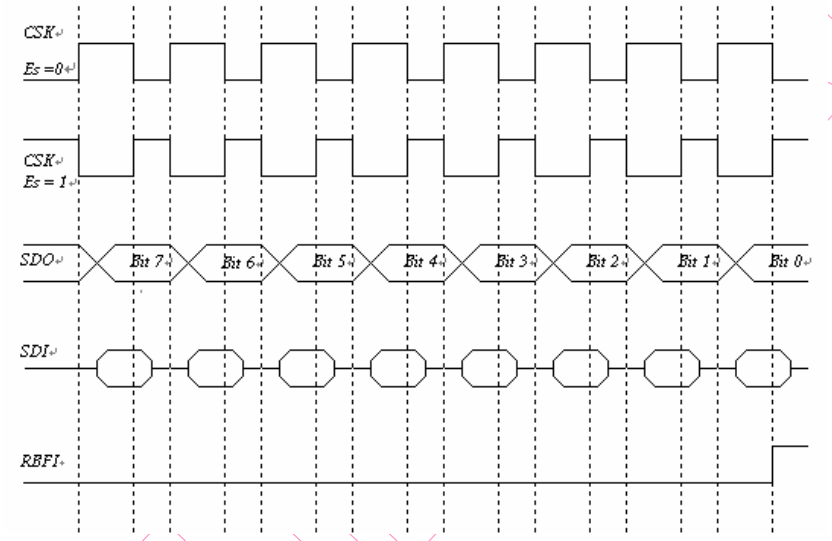


Fig. 6-12 SPI Mode with /SS Disabled

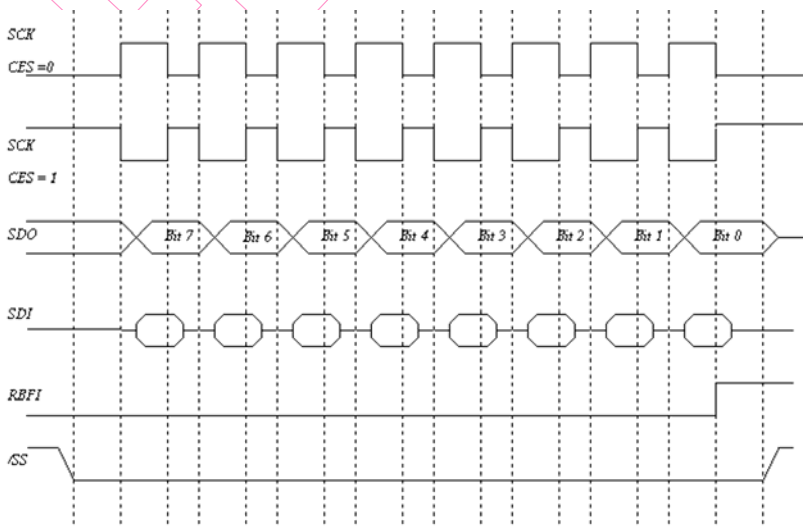


Fig. 6-13 SPI Mode with /SS Enable

6.5.6 SPI Software Application

```
;for master
SPIRB == 0X0A
SPIWB == 0X0B
SPIS == 0X0C
RBF == 0
SCK_OD == 2
SDO_OD == 3
TD0 == 5
TD1 == 6
DORD == 7
SPIC == 0X0D
SBRS0 == 0
SBRS1 == 1
SBRS2 == 2
SDOC == 3
SSE == 4
SRO == 5
SPIE == 6
CES == 7
TC4CR == 0X09
TM4P0 == 0
TM4P1 == 1
TM4E == 2
TM4IF == 4
TM4IE == 5
SPIF == 6
SPIE == 7
ORG  0X00                ; reset vector
JMP  INITIAL
ORG  0X08                ; SPI interrupt vector
BANK 0
IOR   TC4CR
AND   A,@0B10111111
IOW   TC4CR              ; Clear SPI interrupt flag
RETI
ORG  0X50
INITIAL:

MOV  A,@0X80             ; enable SPI interrupt
IOW  TC4CR               ; clear SPI interrupt flag
MOV A,@0X55
MOV  SPIWB,A             ; Transmit data
BS   SPIC,SPIE           ; SPI shift enable bit
BC  SPIS,DORD            ; shift left
BC  SPIS,TD0
BC  SPIS,TD1             ; SDO status output delay times:8 clocks
BC  SPIC,CES             ; rising edge
BC  SPIC,SBRS0
BC  SPIC,SBRS1
BC  SPIC,SBRS2           ; set baud rate: Fc/2
BC  SPIC,SDOC            ; SDO output status control bit: high
ENI                      ; enable interrupt
MAIN:
BS    SPIC,SSE           ; SPI start transmit
JBC   SPIC,SSE
JMP   $-1
NOP
NOP
MOV  A,@0X55             ; transmit data
MOV  SPIWB,A
NOP
NOP
JMP MAIN
```

```
;for slave
PORT7 == 0X07
SPIRB == 0X0A
SPIWB == 0X0B
SPIS == 0X0C
RBF == 0
SCK_OD == 2
SDO_OD == 3
TD0 == 5
TD1 == 6
DORD == 7
SPIC == 0X0D
SBRS0 == 0
SBRS1 == 1
SBRS2 == 2
SDOC == 3
SSE == 4
SRO == 5
SPIE == 6
CES == 7
IOC7 == 0X07
TC4CR == 0X09
TM4P0 == 0
TM4P1 == 1
TM4E == 2
TM4IF == 4
TM4IE == 5
SPIF == 6
SPIE == 7
ORG  0X00                ; reset vector
JMP  INITIAL
 ORG  0X08               ; SPI interrupt vector
 BANK 0
IOR   TC4CR
AND   A,@0B10111111
IOW   TC4CR              ; Clear SPI interrupt flag
RETI
ORG  0X50
INITIAL:
MOV  A,@0X00
IOW   IOC7               ; set port7 as output
MOV  PORT7,A
MOV  A,@0X80             ; enable SPI interrupt
IOW  TC4CR               ; clear SPI interrupt flag
BS   SPIC,SPIE           ; SPI shift enable bit
BC  SPIS,DORD            ; shift left
BC  SPIS,TD0
BC  SPIS,TD1             ; SDO status output delay times:8 clocks
BC  SPIC,CES             ; rising edge
BC  SPIS,DORD            ; shift left
BS  SPIC,SBRS0
BC  SPIC,SBRS1
BS  SPIC,SBRS2           ; set baud rate: /SS enable
BC SPIC,SDOC             ; SDO output status control bit: High
ENI
MIAN:
BS    SPIC,SSE           ; SPI start transmit
JBS   SPIS,RBF           ; determine data receive finish
JMP   $-1
JBC   SPIC,SRO           ; determine data overflow
JMP   MAIN
MOV  A,SPIRB             ; receive data
MOV  PORT7,A
NOP
JMP  MAIN
```

6.6 Timer 4

6.6.1 Overview

Timer 4 (TMR4) is an 8-bit clock up-counter with a programmable prescaler. When TMR4 is in SPI baud rate clock generator mode (SBRS0, SBRS1 and SBRS2 are set to 1) and SPI control register Bit 4 (SSE) is set to 1, Timer 4 will enable automatically without setting TM4E. TMR4 can be read and written to and cleared on any reset conditions.

6.6.2 Function Description

Fig. 6-14 shows Timer 4 block diagram. Each signal and block is described as follows:

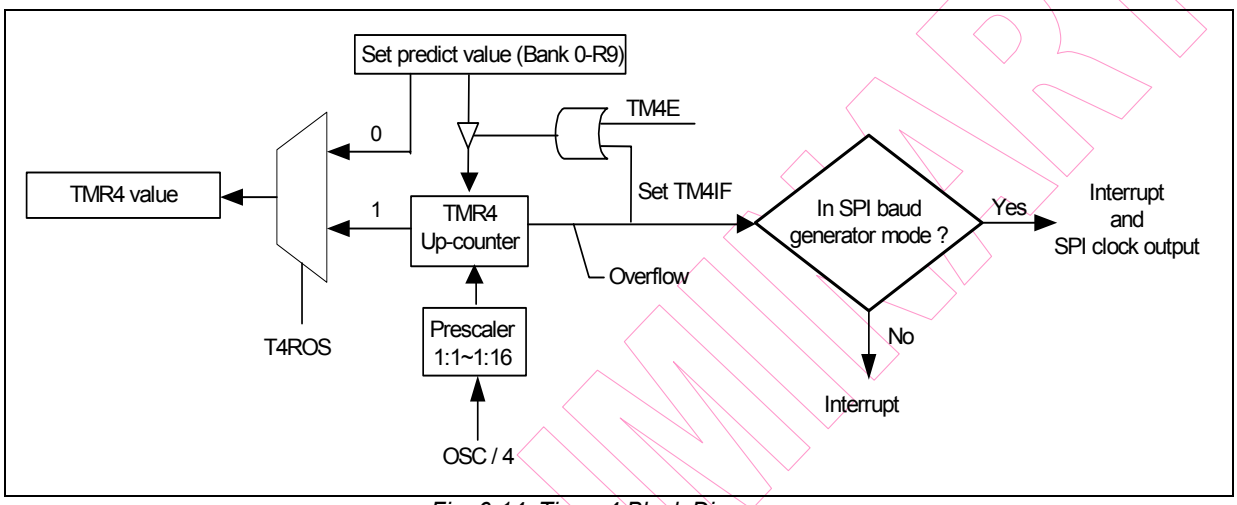


Fig. 6-14 Timer 4 Block Diagram

- OSC/4: Input clock.
- Prescaler: Option 1:1, 1:4, 1:8, and 1:16 defined by TM4P1 and TM4P2 (T4CON<1, 0>). It is cleared when a value is written to TMR4 or T4CON, and during any kind of reset as well.
- TMR4: Timer 4 register. TMR4 is incremented until it overflows, and then resets to 0. If it is in the SPI baud rate generator mode, its output is fed as a shifting clock. TMR4 register; increases until it overflows, and then reloads the predicted value. If writing a value to Timer 4, the predicted value and TMR4 value will be the set value. However, if T4ROS is set to 1 and read value from TMR4, the value will be TMR4 direct value, else T4ROS is set to 0 and read value from TMR4, the value will be TMR4 predicted value.

6.6.3 Programming the Related Registers

The related registers of the defined TMR4 operation are shown in Table 4 and Table 5

Table 3 TMR4 Related Control Registers

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0C	SPIS/RC (Bank 0)	DORD	TD1	TD0	T4ROS	OD3	OD4	–	RBF
NA	T4CR/IOC9	SPIE	SPIF	TM4IE	TM4IF	"0"	TM4E	TM4P1	TM4P0

Table 4 Related Status/Data Registers ofTMR4

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x09	TMR4/R9 (Bank 0)	TMR47	TMR46	TMR45	TMR44	TMR43	TMR42	TMR41	TMR40
NA	T4CR/IOC9	SPIE	SPIF	–	TM4IF	"0"	TM4E	TM4P1	TM4P0

TMR4: Timer 4 Register

TMR47~TMR40 are set of Timer 4 register bits which are incremented until the value matches PWP and then resets to 0.

T4ROS (Bit 4): Timer 4 Read Buffer Select Bit

0 : Read Value from Timer 4 Preset Register

1 : Read Value from Timer 4 Counter Register

T4CR: Timer 4 Control Register

Bit 2 (TM4E): Timer4 enable bit

Bit 1 (TM4P1) and Bit 0 (TM4P): Timer 4 prescaler for FSCO

TM4P1	TM4P0	Prescaler Rate
0	0	1:1
0	1	1:4
1	0	1:8
1	1	1:16

6.7 Reset and Wake-up

6.7.1 Reset and Wake-up Operation

A Reset is initiated by one of the following events:

1. Power-on reset
2. /RESET pin input "low"
3. WDT time-out (if enabled)

A device is kept in a reset condition for the duration of approximately 18ms.[2] after the reset is detected. When in LXT mode, the reset time is 500ms. Once a reset occurs, the following functions are performed (the initial address is 000h):

- The oscillator continues running, or will be started (if in sleep mode).
- The Program Counter (R2) is set to all "0".
- All I/O port pins are configured as input mode (high-impedance state).
- The Watchdog Timer and prescaler are cleared.
- When power is switched on, the upper 3 bits of R3 and upper 2 bits of R4 are cleared.
- The CONT register bits are set to all "0".

Executing the “SLEP” instruction will assert the sleep (power down) mode. While entering sleep mode, the Oscillator, TCC, Timer 1, Timer 2, and Timer 3 are stopped. The WDT (if enabled) is cleared but keeps on running.

The controller can be awakened by:

Case 1 External reset input on /RESET pin

Case 2 WDT time-out (if enabled)

Case 3 Port 6 input status changes (if ICWE is enabled)

Case 4 Comparator output status changes (if CMPWE is enabled)

Case 5 AD conversion completed (if ADWE enable)

Case 6 PWM/Timer overflows (if PWMWE enable)

The first two cases (1 & 2) will cause the EM78P350N to reset. The T and P flags of R3 can be used to determine the source of the reset (wake-up). Cases 3, 4, & 5 are considered the continuation of program execution and the global interrupt ("ENI" or "DISI" being executed) decides whether or not the controller branches to the interrupt vector following wake-up. If ENI is executed before SLEP, the instruction will begin to execute from address 0x8 after wake-up. If DISI is executed before SLEP, the execution will restart from the instruction next to SLEP after wake-up. All sleep mode wake up time is 2ms in high Crystal mode. In RC mode (IRC or ERC), wake-up time is 10μs. In low Crystal mode, wake-up time is 500ms.

[2] VDD=5V, WDT Time-out period = 16.5ms ± 30%.
VDD=3V, WDT Time-out period = 18ms ± 30%.

Only one of Cases 1 to 5 can be enabled before entering into sleep mode. That is:

Case [a] If WDT is enabled before SLEP, all of the RE bit is disabled. Hence, the EM78P350N can be awakened only with Case 1 or Case 2. Refer to the section on Interrupt (Section 6.7) for further details.

Case [b] If Port 6 Input Status Change is used to wake -up the EM78P350N and ICWE bit of RE register is enabled before SLEP, WDT must be disabled. Hence, the EM78P350N can be awakened only with Case 3. Wake-up time is dependent on oscillator mode. In RC mode the reset time is 32 clocks (for stable oscillators).

In High Crystal mode, reset time is 2ms and 32 clocks (for stable oscillators); and in low Crystal mode, the reset time is 500ms.

Case [c] If Comparator output status change is used to wake-up the EM78P350N and the CMPWE bit of the RE register is enabled before SLEP, WDT must be disabled by software. Hence, the EM78P350N can be awakened only with Case 4.

Wake-up time is dependent on oscillator mode. In RC mode, the reset time is 32 clocks (for stable oscillators). In High crystal mode, reset time is 2ms and 32 clocks (for stable oscillators), and in low crystal mode, the reset time is 500ms.

Case [d] If AD conversion completed is used to wake-up the EM78P350N and the ADWE bit of the RE register is enabled before SLEP, WDT must be disabled by software. Hence, the EM78P350N can be awakened only with Case 5. The wake-up time is 15 TAD (ADC clock period).

Wake-up time is dependent on oscillator mode. In RC mode, the reset time is 32 clocks (for stable oscillators). In High crystal mode, reset time is 2ms and 32 clocks (for stable oscillators); and in low crystal mode, the reset time is 500ms.

Case [e] If PWM/Timer output status change is used to wake-up the EM78P350N and the PWMWE bit of the RE register is enabled before Idle mode (except in sleep mode), WDT must be disabled by software. Hence, the EM78P350N can be awakening only with Case 6.

Wake-up time is dependent on the oscillator mode. In RC mode the reset time is 32 clocks (for stable oscillators). In High crystal mode, reset time is 2ms and 32 clocks (for stable oscillators); and in low crystal mode, the reset time is 500ms.

If Port 6 Input Status Change Interrupt is used to wake up the EM78P350N (as in Case b above), the following instructions must be executed before SLEP:

```
MOV           A, @001111xxb     ; Select WDT prescaler and Disable WDT
IOW           IOCE0
WDTC                            ; Clear WDT and prescaler
MOV           R6, R6            ; Read Port 6
ENI (or DISI)                   ; Enable (or disable) global interrupt
MOV           A, @00000x1xb     ; Enable Port 6 input change wake-up bit
MOV           RE
MOV           A, @00000x1xb     ; Enable Port 6 input change interrupt
IOW           IOCF
SLEP                            ; Sleep
```

Similarly, if the Comparator Interrupt is used to wake up the EM78P350N (as in Case [c] above), the following instructions must be executed before SLEP:

```
MOV           A, @xxxxxx10b   ; Select an comparator and P60 act as CO
                                pin
IOW           IOCA0
MOV           A, @001111xxb   ; Select WDT prescaler and Disable WDT
IOW           IOCE0
WDTC                          ; Clear WDT and prescaler
ENI (or DISI)                 ; Enable (or disable) global interrupt
MOV           A, @000001xxb   ; Enable comparator output status change
                                wake-up bit
MOV           RE
MOV           A, @xxxx1xxxb   ; Enable comparator output status change
                                interrupt
IOW           IOCA
SLEP                          ; Sleep
```

6.7.1.1 Wake-up and Interrupt Mode Operation Summary

All categories under Wake-up and Interrupt modes are summarized below.

Signal	Sleep Mode	Idle Mode	Normal Mode
TCC Over Flow	N/A	N/A	DISI + IOCF (TCIE) Bit 0 = 1 Next Instruction+ Set RF (TCIF) = 1 ENI + IOCF (TCIE) Bit 0 = 1 Interrupt Vector (0x08)+ Set RF (TCIF) = 1
Port 6 Input Status Change	RE (ICWE) Bit 1 = 0, IOCF (ICIE) Bit 1 = 0 Oscillator, TCC and TIMERX are stopped. Port 6 input status changed wake-up is invalid.	RE (ICWE) Bit 1 = 0, IOCF (ICIE) Bit 1 = 0 Oscillator, TCC and TIMERX are stopped. Port 6 input status changed wake-up is invalid.	IOCF (ICIE) Bit 1 = 0 Port 6 input status change interrupted is invalid
	RE (ICWE) Bit 1 = 0, IOCF (ICIE) Bit 1 = 1 Set RF (ICIF) = 1, Oscillator, TCC and TIMERX are stopped. Port 6 input status changed wake-up is invalid.	RE (ICWE) Bit 1 = 0, IOCF (ICIE) Bit 1 = 1 Set RF (ICIF) = 1, Oscillator, TCC and TIMERX are stopped. Port 6 input status changed wake-up is invalid.	
	RE (ICWE) Bit 1 = 1, IOCF (ICIE) Bit 1 = 0 Wake-up+ Next Instruction Oscillator, TCC and TIMERX are stopped.	RE (ICWE) Bit 1 = 1, IOCF (ICIE) Bit 1 = 0 Wake-up+ Next Instruction Oscillator, TCC and TIMERX are stopped.	
	RE (ICWE) Bit 1 = 1, DISI + IOCF (ICIE) Bit 1 = 1 Wake-up+ Next Instruction+ Set RF (ICIF) = 1 Oscillator, TCC and TIMERX are stopped.	RE (ICWE) Bit 1 = 1, DISI + IOCF (ICIE) Bit 1 = 1 Wake-up + Next Instruction + Set RF (ICIF) = 1 Oscillator, TCC and TIMERX are stopped.	DISI + IOCF (ICIE) Bit 1 = 1 Next Instruction + Set RF (ICIF) = 1
	RE (ICWE) Bit 1 = 1, ENI + IOCF (ICIE) Bit 1 = 1 Wake-up+ Interrupt Vector (0x08)+ Set RF (ICIF) = 1 Oscillator, TCC and TIMERX are stopped.	RE (ICWE) Bit1=1, ENI + IOCF (ICIE) Bit 1 = 1 Wake-up+ Interrupt Vector (0x08)+ Set RF (ICIF) = 1 Oscillator, TCC and TIMERX are stopped.	ENI + IOCF (ICIE) Bit 1 = 1 Interrupt Vector (0x08)+ Set RF (ICIF) = 1
INT Pin	N/A	N/A	DISI + IOCF (EXIE1, 0) Bit 2, 3 = 1 Next Instruction+ Set RF (EXIF)=1 ENI + IOCF (EXIE1, 0) Bit 2, 3 = 1 Interrupt Vector (0x08)+ Set RF (EXIF) = 1
AD Conversion	RE (ADWE) Bit 3 = 0, IOCF (ADIE) Bit 4 = 0 Clear Bank 1-R9 (ADRUN)=0, ADC is stopped, AD conversion wake-up is invalid. Oscillator, TCC and TIMERX are stopped.	RE (ADWE) Bit 3 = 0, IOCF (ADIE) Bit 4 = 0 Clear Bank 1-R9 (ADRUN)=0, ADC is stopped, AD conversion wake-up is invalid. Oscillator, TCC and TIMERX are stopped.	IOCF (ADIE) Bit 1 = 0 AD conversion interrupted is invalid
	RE (ADWE) Bit 3 = 0, IOCF (ADIE) Bit 4 = 1 Set RF (ADIF)=1, Bank 1-R9 (ADRUN) = 0, ADC is stopped AD conversion wake-up is invalid. Oscillator, TCC and TIMERX are stopped.	RE (ADWE) Bit 3 = 0, IOCF (ADIE) Bit 4 = 1 Set RF (ADIF) = 1, Bank 1-R9 (ADRUN) = 0, ADC is stopped, AD conversion wake-up is invalid. Oscillator, TCC and TIMERX are stopped.	
	RE (ADWE) Bit 3 = 1, IOCF (ADIE) Bit 4 = 0 Wake-up+ Next Instruction, Oscillator, TCC and TIMERX keep on running. Wake-up when ADC completed.	RE (ADWE) Bit 3 = 1, IOCF (ADIE) Bit 4 = 0 Wake-up+ Next Instruction, Oscillator, TCC and TIMERX keep on running. Wake-up when ADC completed.	

Signal	Sleep Mode	Idle Mode	Normal Mode
AD Conversion	RE (ADWE) Bit 3 = 1, DISI + IOCF (ADIE) Bit 4 = 1	RE (ADWE) Bit 3 = 1, DISI + IOCF (ADIE) Bit 4 = 1	DISI + IOCF (ADIE) Bit 4=1
	Wake-up+ Next Instruction+ RF (ADIF) = 1, Oscillator, TCC and TIMERX keep on running. Wake-up when ADC completed.	Wake-up+ Next Instruction+ RF (ADIF) = 1, Oscillator, TCC and TIMERX keep on running. Wake-up when ADC completed.	Next Instruction+ RF (ADIF)=1
	RE (ADWE) Bit 3 = 1, ENI + IOCF (ADIE) Bit 4 = 1	RE (ADWE) Bit 3 = 1, ENI + IOCF (ADIE) Bit 4 = 1	ENI + IOCF (ADIE) Bit 4 = 1
	Wake-up+ Interrupt Vector (0x08)+ RF (ADIF) = 1, Oscillator, TCC and TIMERX keep on running. Wake-up when ADC completed.	Wake-up+ Interrupt Vector (0x08)+ RF (ADIF) = 1, Oscillator, TCC and TIMERX keep on running. Wake-up when ADC completed.	Interrupt Vector (0x08)+ Set RF (ADIF) = 1
PWMX (PWM1, PWM2, PWM3) (When TimerX matches PRDX)	N/A	RE (PWMWE) = 0, IOCA (PWMIE) bit 0 = 0, if TxS = 1	DISI + IOCF (PWMXIE) = 1
		Only sub-clock oscillate. PWM wake-up is invalid.	Next Instruction+ Set RF (PWMXIF) = 1
		RE (PWMWE) = 0, IOCA (PWMIE) Bit 0 = 1, if TxS = 1	ENI + IOCF (PWMXIE) = 1
		Set PWMIF = 1 Only sub-clock oscillate. PWM wake-up is invalid.	
		RE (PWMWE) = 1, IOCA (PWMIE) Bit 0 = 1, if TxS = 0	
		Wake-up+ Next Instruction, Only sub-clock oscillate.	
		RE (PWMWE) = 1, IOCA (PWMIE) Bit 0 = 1, DISI, if TxS = 1	
		Wake-up+ Next Instruction, Only sub-clock oscillate.	
		RE (PWMWE) = 1, IOCA (PWMIE) Bit 0 = 1, ENI, if TxS = 1	
		Wake-up+ Interrupt Vector (0x08)+ Set RF (PWMIF) = 1 Only sub-clock oscillate.	Interrupt Vector (0x08)+ Set RF (PWMXIF) = 1
Comparator (Comparator Output Status Change)	RE (CMPWE) Bit 2 = 0, IOCE (CMPIE) Bit 0 = 0	RE (CMPWE) Bit 2 = 0, IOCE (CMPIE) Bit 0 = 0	IOCF (CMPIE) Bit 7 = 0
	Comparator output status changed wake-up is invalid. Oscillator, TCC and TIMERX are stopped.	Comparator output status changed wake-up is invalid. Oscillator, TCC and TIMERX are stopped.	Comparator output status change interrupted is invalid.
	RE (CMPWE) Bit 2 = 0, IOCE (CMPIE) Bit 0 = 1	RE (CMPWE) Bit 2 = 0, IOCE (CMPIE) Bit 0 = 1	
	Set RF (CMPIF) = 1, Comparator output status changed wake-up is invalid. Oscillator, TCC and TIMERX are stopped.	Set RF (CMPIF) = 1, Comparator output status changed wake-up is invalid. Oscillator, TCC and TIMERX are stopped.	
	RE (CMPWE) Bit 2 = 1, IOCE (CMPIE) Bit 0 = 0	RE (CMPWE) Bit 2 = 1, IOCE (CMPIE) Bit 0 = 0	
	Wake-up+ Next Instruction, Oscillator, TCC and TIMERX are stopped.	Wake-up+ Next Instruction, Oscillator, TCC and TIMERX are stopped.	
	RE (CMPWE) Bit 2 = 1, DISI + IOCE (CMPIE) Bit 0 = 1	RE (CMPWE) Bit 2 = 1, DISI + IOCE (CMPIE) Bit 0 = 1	DISI + IOCE (CMPIE) Bit 0 = 1
	Wake-up+ Next Instruction+ Set RF (CMPIF) = 1, Oscillator, TCC and TIMERX are stopped.	Wake-up+ Next Instruction+ Set RF (CMPIF) = 1, Oscillator, TCC and TIMERX are stopped.	Next Instruction+ Set RF (CMPIF) = 1
	RE (CMPWE) Bit 2 = 1, ENI + IOCE (CMPIE) Bit 0 = 1	RE (CMPWE) Bit 2 = 1, ENI + IOCE (CMPIE) Bit 0 = 1	ENI + IOCE (CMPIE) Bit 0 = 1
	Wake-up+ Interrupt Vector (0x08)+ Set RF (CMPIF) = 1, Oscillator, TCC and TIMERX are stopped.	Wake-up+ Interrupt Vector (0x08)+ Set RF (CMPIF) = 1, Oscillator, TCC and TIMERX are stopped.	Interrupt Vector (0x08)+ Set RF (CMPIF) = 1
WDT Time Out IOCE (WDTE) Bit 7 = 1	Wake-up+ Reset (Address 0x00)	Wake-up+ Reset (Address 0x00)	Reset (Address 0x00)

6.7.1.2 Register Initial Values after Reset

The following summarizes the registers initialized values.

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
N/A	IOC5	Bit Name	C57	C56	C55	C54	C53	C52	C51	C50
		Power-on	1	1	1	1	1	1	1	1
		/RESET & WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin change	P	P	P	P	P	P	P	P
N/A	IOC6	Bit Name	C67	C66	C65	C64	C63	C62	C61	C60
		Power-on	1	1	1	1	1	1	1	1
		/RESET & WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin change	P	P	P	P	P	P	P	P
N/A	IOC7	Bit Name	C77	C76	C75	C74	C73	C72	C71	C70
		Power-on	1	1	1	1	1	1	1	1
		/RESET & WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin change	P	P	P	P	P	P	P	P
N/A	IOC8	Bit Name	-	-	-	C84	C83	C82	C81	C80
		Power-on	0	0	0	1	1	1	1	1
		/RESET &WDT	0	0	0	1	1	1	1	1
		Wake-up from Pin change	P	P	P	P	P	P	P	P
N/A	IOC9 (T4CR)	Bit Name	SPIE	SPIF	TM4IF	TM4IE	-	TM4E	TM4P1	TM4P0
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin change	P	P	P	P	P	P	P	P
N/A	IOCA (CMPCON)	Bit Name	-	-	-	CMPIF	CMPIE	CPOUT	COS1	COS0
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin change	P	P	P	P	P	P	P	P
N/A	IOCC	Bit Name	-	-	-	-	-	-	-	-
		Power-on	1	1	1	1	1	1	1	1
		/RESET & WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin change	P	P	P	P	P	P	P	P
N/A	IOCD	Bit Name	-	-	-	-	-	-	-	-
		Power-on	1	1	1	1	1	1	1	1
		/RESET & WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin change	P	P	P	P	P	P	P	P

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
N/A	IOCE	Bit Name	WDTE	EIS0	EIS1	PSWE	PSW2	PSW1	PSW0	LVDIE
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin change	P	P	P	P	P	P	P	P
N/A	IOCF	Bit Name	PMW3IE	PMW2IE	PWM1IE	ADIE	EXIE1	EXIE0	ICIE	TCIE
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin change	P	P	P	P	P	P	P	P
N/A	CONT	Bit Name	INTE	INT	TS	TE	PSTE	PST2	PST1	PST0
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin change	P	P	P	P	P	P	P	P
0x00	R0(IAR)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	U	U	U	U	U	U	U	U
		/RESET & WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin change	P	P	P	P	P	P	P	P
0x01	R1(TCC)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin change	P	P	P	P	P	P	P	P
0x02	R2(PC)	Bit Name	-	-	-	-	-	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin Change	Jump to address 0x08 or continue to execute next instruction							
0x03	R3(SR)	Bit Name	PS2	PS1	PS0	T	P	Z	DC	C
		Power-on	0	0	0	1	1	U	U	U
		/RESET & WDT	0	0	0	t	t	P	P	P
		Wake-up from Pin change	P	P	P	t	t	P	P	P
0x04	R4(RSR)	Bit Name	RBS1	RBS0	-	-	-	-	-	-
		Power-on	0	0	U	U	U	U	U	U
		/RESET & WDT	0	0	P	P	P	P	P	P
		Wake-up from Pin change	P	P	P	P	P	P	P	P
0x05	P5	Bit Name	P57	P56	P55	P54	P53	P52	P51	P50
		Power-on	U	U	U	U	U	U	U	U
		/RESET & WDT	U	U	U	U	U	U	U	U
		Wake-up from Pin change	P	P	P	P	P	P	P	P

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x06	P6	Bit Name	P67	P66	P65	P64	P63	P62	P61	P60
		Power-on	U	U	U	U	U	U	U	U
		/RESET & WDT	U	U	U	U	U	U	U	U
		Wake-up from Pin change	P	P	P	P	P	P	P	P
0x7	P7	Bit Name	P74	P73	P72	P74	P73	P72	P71	P70
		Power-on	U	U	U	U	U	U	U	U
		/RESET & WDT	U	U	U	U	U	U	U	U
		Wake-up from Pin change	P	P	P	P	P	P	P	P
0x8	P8	Bit Name	“0”	“0”	“0”	P84	P83	P82	P81	P80
		Power-on	U	U	U	U	U	U	U	U
		/RESET & WDT	U	U	U	U	U	U	U	U
		Wake-up from Pin change	P	P	P	P	P	P	P	P
0x9	R9 (T4R)	Bit Name	TMR47	TMR46	TMR45	TMR44	TMR43	TMR42	TMR41	TMR40
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin change	P	P	P	P	P	P	P	P
0xA	RA (SPIR)	Bit Name	SRB7	SRB6	SRB5	SRB4	SRB3	SRB2	SRB1	SRB0
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	U	U	U	U	U	U	U	U
		Wake-up from Pin change	P	P	P	P	P	P	P	P
0xB	RB (SPIW)	Bit Name	SWB7	SWB6	SWB5	SWB4	SWB3	SWB2	SWB1	SWB0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin change	P	P	P	P	P	P	P	P
0xC	RC (SPISB)	Bit Name	DORD	TD1	TD0	T4ROS	OD3	OD4	“0”	RBF
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin change	P	P	P	P	P	P	P	P
0xD	RD (SPICB)	Bit Name	CES	SPIE	SDO	SSE	SDOC	SBRS2	SBRS1	SBRS0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin change	P	P	P	P	P	P	P	P

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0xE	RE (WUCR)	Bit Name	-	-	-	LVDIF	ADWE	CMPWE	ICWE	PWMWE
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin change	P	P	P	P	P	P	P	P
0xF	RF (ISR)	Bit Name	PWM3IF	PWM2IF	PWM1IF	ADIF	EXIF0	EXIF1	ICIF	TCIF
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin change	P	P	P	P	P	P	P	P
0X5	R5 (Bank1)	Bit Name	PWM3E	PWM2E	PWM1E	“0”	T1EN	T1P2	T1P1	T1P0
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin change	P	P	P	P	P	P	P	P
0X6	R6 (Bank 1)	Bit Name	T2EN	T2P2	T2P1	T2P0	T3EN	T3P2	T3P1	T3P0
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin change	P	P	P	P	P	P	P	P
0X7	R7 (Bank 1)	Bit Name	“0”	“0”	“0”	“0”	T2TS	T2TE	T1TS	T1TE
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin change	P	P	P	P	P	P	P	P
0X8	R8 (Bank 1)	Bit Name	PRD1[9]	PRD1[8]	PRD1[7]	PRD1[6]	PRD1[5]	PRD1[4]	PRD1[3]	PRD1[2]
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin change	P	P	P	P	P	P	P	P
0X9	R9 (Bank 1)	Bit Name	PRD2[9]	PRD2[8]	PRD2[7]	PRD2[6]	PRD2[5]	PRD2[4]	PRD2[3]	PRD2[2]
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin change	P	P	P	P	P	P	P	P
0XA	RA (Bank 1)	Bit Name	PRD3[9]	PRD3[8]	PRD3[7]	PRD3[6]	PRD3[5]	PRD3[4]	PRD3[3]	PRD3[2]
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin change	P	P	P	P	P	P	P	P

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0XB	RB (Bank 1)	Bit Name	"0"	"0"	PRD3[1]	PRD3[0]	PRD2[1]	PRD2[0]	PRD1[1]	PRD1[0]
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin change	P	P	P	P	P	P	P	P
0XC	RC (Bank 1)	Bit Name	DT1[9]	DT1[8]	DT1[7]	DT1[6]	DT1[5]	DT1[4]	DT1[3]	DT1[2]
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin change	P	P	P	P	P	P	P	P
0XD	RD (Bank 1)	Bit Name	DT2[9]	DT2[8]	DT2[7]	DT2[6]	DT2[5]	DT2[4]	DT2[3]	DT2[2]
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin change	P	P	P	P	P	0	P	P
0xE	RE (Bank 1)	Bit Name	DT3[9]	DT3[8]	DT3[7]	DT3[6]	DT3[5]	DT3[4]	DT3[3]	DT3[2]
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin change	P	P	P	P	P	0	P	P
0xF	RF (Bank 1)	Bit Name	-	-	DT3[1]	DT3[0]	DT2[1]	DT2[0]	DT1[1]	DT1[0]
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin change	P	P	P	P	P	P	P	P
0X6	R6 (BOCR, Bank 2)	Bit Name	TEN	TCK1	TCK0	FSCS	"0"	"0"	"0"	"0"
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin change	P	P	P	P	P	P	P	P
0X7	R7 (SCR, Bank 2)	Bit Name	T1S	T2S	T3S	"0"	"0"	"0"	"0"	CPUS
		Power-on	0	0	0	0	0	0	0	1
		/RESET & WDT	0	0	0	0	0	0	0	1
		Wake-up from Pin change	P	P	P	P	P	P	P	P
0x8	R8 (AISR, Bank 2)	Bit Name	ADE7	ADE6	ADE5	ADE4	ADE3	ADE2	ADE1	ADE0
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin change	P	P	P	P	P	P	P	P

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x9	R9 (ADCON, Bank 2)	Bit Name	VREFS	CKR1	CKR0	ADRUN	ADPD	ADIS2	ADIS1	ADIS0
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin change	P	P	P	P	P	P	P	P
0xA	RA (ADOC, Bank 2)	Bit Name	CALI	SIGN	VOF[2]	VOF[1]	VOF[0]	-	-	-
		Power-on	0	0	0	0	0	0	0	0
		/RESET and WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin change	P	P	P	P	P	P	P	P
0xB	RB (ADDDATA, Bank 2)	Bit Name	AD11	AD10	AD9	AD8	AD7	AD6	AD5	AD4
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	U	U	U	U	U	U	U	U
		Wake-up from Pin change	P	P	P	P	P	P	P	P
0xC	RC (ADDATA1H, Bank 2)	Bit Name	-	-	-	-	AD11	AD10	AD9	AD8
		Power-on	0	0	0	0	U	U	U	U
		/RESET and WDT	0	0	0	0	U	U	U	U
		Wake-up from Pin change	P	P	P	P	P	P	P	P
0XD	RD (ADDATA1L, Bank 2)	Bit Name	AD7	AD7	AD5	AD4	AD3	AD2	AD1	AD0
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	U	U	U	U	U	U	U	U
		Wake-up from Pin change	P	P	P	P	P	P	P	P
0XE	RE (LVDC, Bank 2)	Bit Name	“0”	“0”	“0”	“0”	LVDEN	/LVD	LVD1	LVD0
		Power-on	0	0	0	0	0	1	0	0
		/RESET and WDT	0	0	0	0	0	1	0	0
		Wake-up from Pin change	P	P	P	P	P	P	P	P
0XF	RF (TIMER3H, Bank 2)	Bit Name	TMR3H[9]	TMR3H[8]	TMR3H[7]	TMR3H[6]	TMR3H[5]	TMR3H[4]	TMR3H[3]	TMR3H[2]
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin change	P	P	P	P	P	P	P	P
0X5	R5 (Bank 3)	Bit Name	/PL57	/PL56	/PL55	/PL54	/PL53	/PL52	/PL51	/PL50
		Power-on	1	1	1	1	1	1	1	1
		/RESET & WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin change	P	P	P	P	P	P	P	P

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0X6	R6 (Bank3)	Bit Name	/PL67	/PL66	/PL65	/PL64	/PL63	/PL62	/PL61	/PL60
		Power-on	1	1	1	1	1	1	1	1
		/RESET & WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin change	P	P	P	P	P	P	P	P
0X7	R7 (Bank3)	Bit Name	/PL77	/PL76	/PL75	/PL74	/PL73	/PL72	/PL71	/PL70
		Power-on	1	1	1	1	1	1	1	1
		/RESET & WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin change	P	P	P	P	P	P	P	P
0X8	R8 (Bank3)	Bit Name	“0”	“0”	“0”	/PL84	/PL83	/PL82	/PL81	/PL80
		Power-on	0	0	0	1	1	1	1	1
		/RESET & WDT	0	0	0	1	1	1	1	1
		Wake-up from Pin change	P	P	P	P	P	P	P	P
0X9	R9 (Bank3)	Bit Name	/PH57	/PH56	/PH55	/PH54	/PH53	/PH52	/PH51	/PH50
		Power-on	1	1	1	1	1	1	1	1
		/RESET & WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin change	P	P	P	P	P	P	P	P
0XA	RA (Bank3)	Bit Name	/PH67	/PH66	/PH65	/PH64	/PH63	/PH62	/PH61	/PH60
		Power-on	1	1	1	1	1	1	1	1
		/RESET & WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin change	P	P	P	P	P	P	P	P
0XB	RB (Bank3)	Bit Name	/PH77	/PH76	/PH75	/PH74	/PH73	/PH72	/PH71	/PH70
		Power-on	1	1	1	1	1	1	1	1
		/RESET & WDT	1	1	1	1	1	1	1	1
		Wake-up from Pin change	P	P	P	P	P	P	P	P
0XC	RC (Bank3)	Bit Name	“0”	“0”	“0”	/PH84	/PH83	/PH82	/PH81	/PH80
		Power-on	0	0	0	1	1	1	1	1
		/RESET & WDT	0	0	0	1	1	1	1	1
		Wake-up from Pin change	P	P	P	P	P	P	P	P
0XD	RD (TMR1H Bank 3)	Bit Name	TMR1H[9]	TMR1H[8]	TMR1H[7]	TMR1H[6]	TMR1H[5]	TMR1H[4]	TMR1H[1]	TMR1H[0]
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin change	P	P	P	P	P	P	P	P

Address	Name	Reset Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0xE	RE (TMR2H, Bank 3)	Bit Name	TMR2H[9]	TMR2H[8]	TMR2H[7]	TMR2H[6]	TMR2H[5]	TMR2H[4]	TMR2H[3]	TMR2H[2]
		Power-on	0	0	0	0	0	0	0	0
		/RESET & WDT	0	0	0	0	0	0	0	0
		Wake-up from Pin change	P	P	P	P	P	P	P	P
0xF	RF(TMRL, Bank 3)	Bit Name	"0"	"0'	TMR3[1]	TMR3[0]	TMR2[1]	TMR2[0]	TMR1[3]	TMR1[2]
		Power-on	0	0	0	1	0	1	0	1
		/RESET & WDT	0	0	0	1	0	1	0	1
		Wake-up from Pin change	P	P	P	P	P	P	P	P
0x10 ~ 0x3F	R10 ~ R3F	Bit Name	-	-	-	-	-	-	-	-
		Power-on	U	U	U	U	U	U	U	U
		/RESET and WDT	P	P	P	P	P	P	P	P
		Wake-up from Pin change	P	P	P	P	P	P	P	P

Legend: **"–"** = not used **"P"** = previous value before reset
"u" = unknown or don't care **"t"** = check "Reset Type" Table in Section 6.5.2

6.7.1.3 Controller Reset Block Diagram

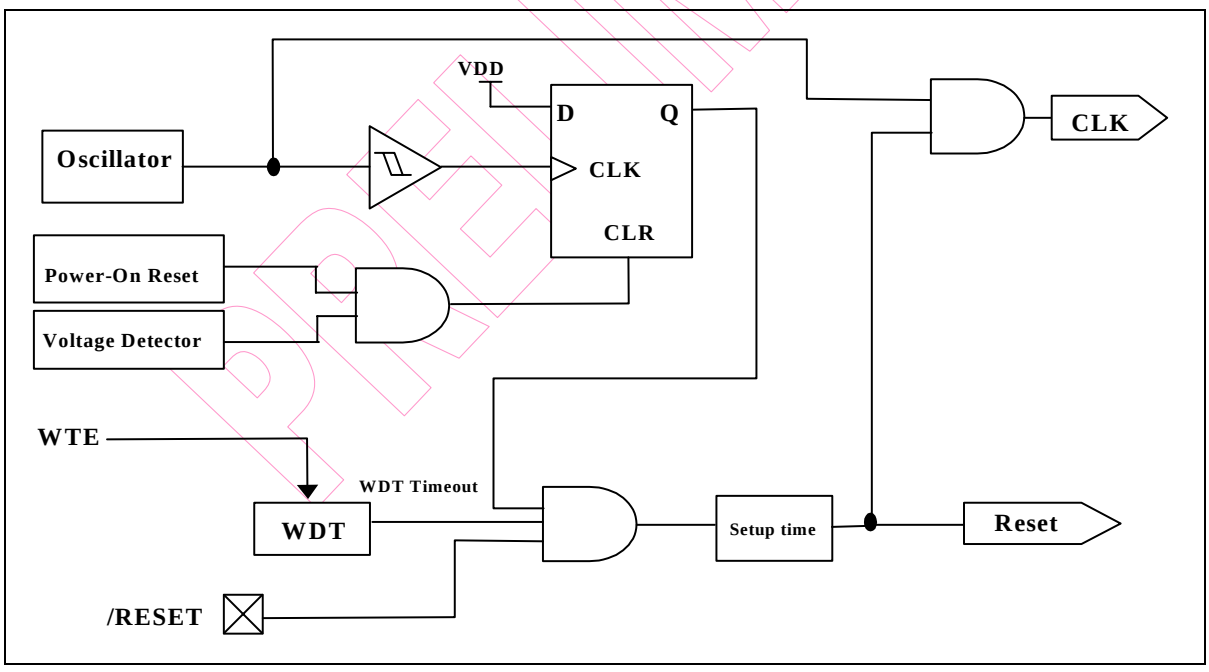


Fig. 6-7 Controller Reset Block Diagram

6.7.2 The T and P Status under Status Register

A reset condition is initiated by one of the following events:

1. Power-on reset
2. /RESET pin input "low"
3. WDT time-out (if enabled)

The values of T and P as listed in the table below, are used to check how the processor wakes up.

Reset Type	T	P
Power-on	1	1
/RESET during Operating mode	*P	*P
/RESET wake-up during Sleep mode	1	0
WDT during Operating mode	0	*P
WDT wake-up during Sleep mode	0	0
Wake-up on pin change during Sleep mode	1	0

*P: Previous status before reset

The following shows the events that may affect the status of T and P.

Event	T	P
Power-on	1	1
WDTC instruction	1	1
WDT time-out	0	*P
SLEP instruction	1	0
Wake-up on pin changed during Sleep mode	1	0

*P: Previous value before reset

6.8 Interrupt

The EM78P350N has seven interrupts as listed below:

1. TCC overflow interrupt
2. Port 6 Input Status Change Interrupt
3. External interrupt [(P52, /INT0), (P53, /INT1) pin]
4. Analog-to-Digital conversion completed
5. When TMR1/TMR2 matches with PRD1/PRD2/PRD3 respectively in PWM
6. When the comparators output changes (for EM78P350N only)
7. Completion of Serial interface transmit/receive

Before the Port 6 Input Status Change Interrupt is enabled, reading Port 6 (e.g., "MOV R6, R6") is necessary. Each Port 6 pin will have this feature if its status changes. Any pin configured as output, including the P52 (/INT0), and P53 (/INT1), is excluded from this function. Port 6 Input Status Change Interrupt will wake up the EM78P350N from sleep mode if it is enabled prior to going into sleep mode by executing SLEP. When wake-up occurs, the controller will continue to execute the succeeding program if the global interrupt is disabled. If enabled, it will branch out to the interrupt vector 008H.

External interrupt with digital noise rejection circuit (input pulse less than 8 system clock cycle) is eliminated as noise. Edge selection is possible with /INT. Refer to Word 1 Bits 8~7 (Section 6.16.2, *Code Option Register (Word 1)*) for digital noise rejection definition.

RF is the interrupt status register that records the interrupt requests in the relative flags/bits. IOCF is an interrupt mask register. The global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction. When one of the interrupts (when enabled) occurs, the next instruction will be fetched from address 008H. Once in the interrupt service routine, the source of an interrupt can be determined by polling the flag bits in RF. The interrupt flag bit must be cleared by instructions before leaving the interrupt service routine to avoid recursive interrupts.

The flag (except ICIF bit) in the Interrupt Status Register (RF) is set regardless of the status of its mask bit or of the ENI execution. Note that the result of RF will be the logic AND of RF and IOCF (refer to the figure below). The RETI instruction ends the interrupt routine and enables the global interrupt (the ENI execution).

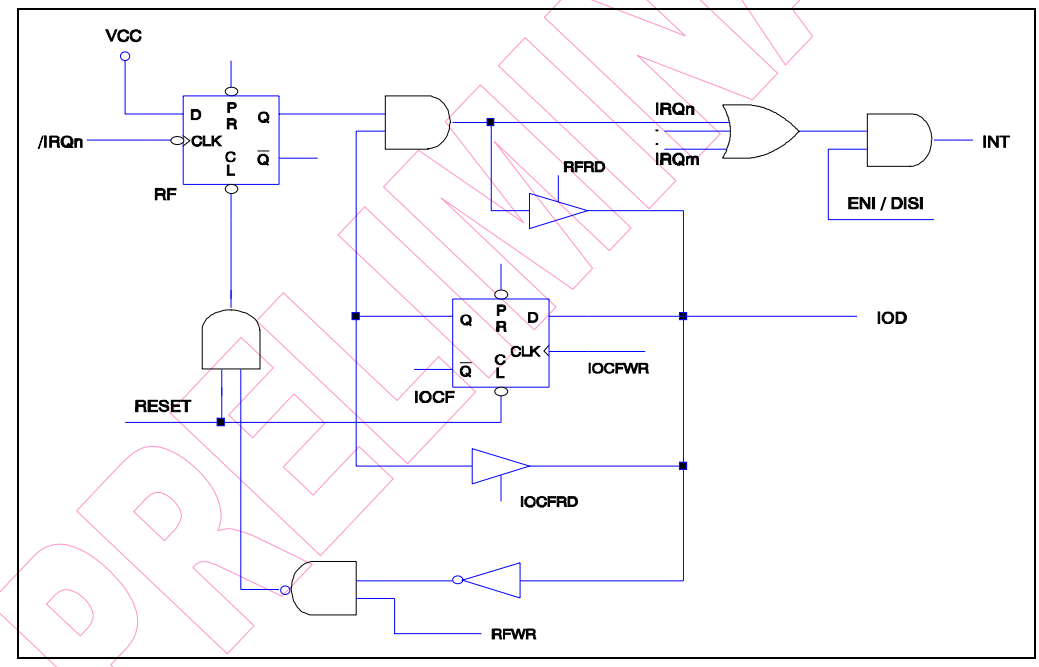


Fig. 6-8 Interrupt Input Circuit

6.9 Analog-to-Digital Converter (ADC)

The analog-to-digital circuitry consists of an 8-bit analog multiplexer; three control registers (AISR/R8, ADCON/R9, & ADOC/RA), three data registers (ADDATA1/RB, ADDATA1H/RC, & ADDATA1L/RD) and an ADC with 12-bit resolution as shown in the functional block diagram below. The analog reference voltage (Vref) and the analog ground are connected via separate input pins.

The ADC module utilizes successive approximation to convert the unknown analog signal into a digital value. The result is fed to the ADDATA, ADDATA1H and ADDATA1L. Input channels are selected by the analog input multiplexer via the ADCON register bits.

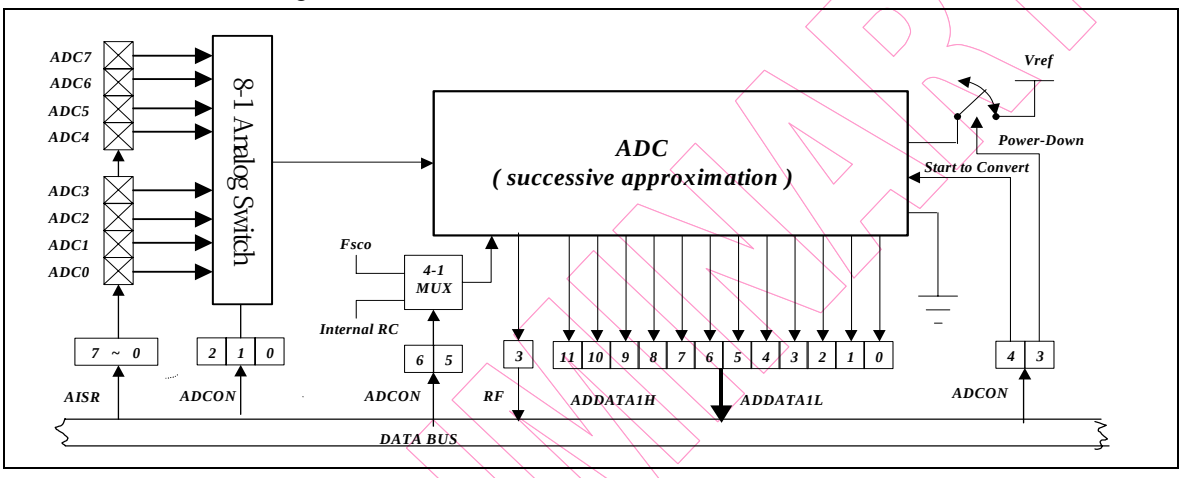


Fig. 6-9 Analog-to-Digital Conversion Functional Block Diagram

6.9.1 ADC Control Register (AISR/Bank 2 R8, ADCON/ Bank 2 R9, ADOC/ Bank 2 RA)

6.9.1.1 Bank 2 R8 (AISR: ADC Input Select Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Symbol	ADE7	ADE6	ADE5	ADE4	ADE3	ADE2	ADE1
*Init_Value	0	0	0	0	0	0	0

*Init_Value: Initial value at power-on reset

The **AISR** register individually defines the Port 6 pins as analog inputs or as digital I/O.

Bit 7 (ADE7): AD converter enable bit of P67 pin
0 = Disable AIN7, P67 functions as I/O pin
1 = Enable AIN7 to function as analog input pin

Bit 6 (ADE6): AD converter enable bit of P66 pin
0 = Disable AIN6, P66 functions as I/O pin
1 = Enable AIN6 to function as analog input pin

Bit 5 (ADE5): AD converter enable bit of P65 pin
0 = Disable AIN5, P65 functions as I/O pin
1 = Enable AIN5 to function as analog input pin

Bit 4 (ADE4): AD converter enable bit of P64 pin

0 = Disable AIN4, P64 functions as I/O pin

1 = Enable AIN4 to function as analog input pin

Bit 3 (ADE3): AD converter enable bit of P63 pin

0 = Disable AIN3, P63 functions as I/O pin

1 = Enable AIN3 to function as analog input pin

Bit 2 (ADE2): AD converter enable bit of P62 pin

0 = Disable AIN2, P63 functions as I/O pin

1 = Enable AIN2 to function as analog input pin

Bit 1 (ADE1): AD converter enable bit of P61 pin

0 = Disable AIN1, P61 functions as I/O pin

1 = Enable AIN1 to function as analog input pin

Bit 0 (ADE0): AD converter enable bit of P60 pin

0 = Disable AIN0, P60 functions as I/O pin

1 = Enable AIN0 to function as analog input pin

NOTE

The P60/AIN0 pin priority is as follows:

P60/ADE0 Priority	
High	**Low**
AIN0	**P60**

6.9.1.2 Bank 2 R9 (ADCON: ADC Control Register)

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Symbol	VREFS	CKR1	CKR0	ADRUN	ADPD	ADIS2	ADIS1	ADIS0
*Init_Value	0	0	0	0	0	0	0	0

*Init_Value: Initial value at power on reset

The **ADCON** register controls the operation of the AD conversion and determines which pin should be currently active.

Bit 7(VREFS): The input source of the ADC Vref

0 = The ADC Vref is connected to Vdd (default value), and the P84/VREF pin carries out the function of P84.

1 = The ADC Vref is connected to P84/VREF.

Bit 6 ~ Bit 5 (CKR1 ~ CKR0): The prescaler oscillator clock rate of ADC

00 = 1:16 (default value)

01 = 1: 4

10 = 1: 64

11 = 1: WDT ring oscillator frequency

CKR1:CKR0	Operation Mode	Max. Operation Frequency
00	Fosc/16	4MHz
01	Fosc/4	1 MHz
10	Fosc/64	16MHz
11	Internal RC	-

Bit 4 (ADRUN): ADC starts to run

0 = reset on completion of the conversion. This bit cannot be reset though software.

1 = an AD conversion is started. This bit can be set by software.

Bit 3 (ADPD): ADC Power-down mode.

0 = switch off the resistor reference to save power even while the CPU is operating.

1 = ADC is operating

Bit 2 ~ Bit 0 (ADIS2 ~ ADIS0): Analog Input Select.

000 = AN0/P60

001 = AN1/P61

010 = AN2/P62

011 = AN3/P63

100 = AN4/P64

101 = AN5/P65

110 = AN6/P66

111 = AN7/P67

These bits can only be changed when the ADIF bit and the ADRUN bit are both low.

6.9.1.3 Bank 2 RA (ADOC: ADC Offset Calibration Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CALI	SIGN	VOF[2]	VOF[1]	VOF[0]	"0"	"0"	"0"

Bit 7 (CALI): Calibration enable bit for ADC offset

0 = disable Calibration

1 = enable Calibration

Bit 6 (SIGN): Polarity bit of offset voltage

0 = Negative voltage

1 = Positive voltage

Bit 5 ~ Bit 3 (VOF[2] ~ VOF[0]): Offset voltage bits

VOF[2]	VOF[1]	VOF[0]	EM78P350N
0	0	0	0LSB
0	0	1	2LSB
0	1	0	4LSB
0	1	1	6LSB
1	0	0	8LSB
1	0	1	10LSB
1	1	0	12LSB
1	1	1	14LSB

Bit 2 ~ Bit 0: Unimplemented, read as '0'.

6.9.2 ADC Data Register (ADDATA/Bank 2 RB, ADDATA1H/Bank 2 RC, ADDATA1L/Bank 2 RD)

When the AD conversion is completed, the result is loaded to the ADDATA, ADDATA1H and ADDATA1L registers. The ADRUN bit is cleared, and the ADIF is set.

6.9.3 ADC Sampling Time

The accuracy, linearity, and speed of the successive approximation of AD converter are dependent on the properties of the ADC and the comparator. The source impedance and the internal sampling impedance directly affect the time required to charge the sample holding capacitor. The application program controls the length of the sample time to meet the specified accuracy. Generally speaking, the program should wait for 2μs for each KΩ of the analog source impedance and at least 2μs for the low-impedance source. The maximum recommended impedance for analog source is 10KΩ at Vdd=5V. After the analog input channel is selected, this acquisition time must be done before the conversion is started.

6.9.4 AD Conversion Time

CKR1 and CKR0 select the conversion time (Tct), in terms of instruction cycles. This allows the MCU to run at a maximum frequency without sacrificing the AD conversion accuracy. For the EM78P350N, the conversion time per bit is 4μs.

The table below shows the relationship between Tct and the maximum operating frequencies.

CKR1: CKR0	Operation Mode	Max. Operation Frequency	Max. Conversion Rate/Bit	Max. Conversion Rate
00	Fosc/16	4MHz	250kHz (4μs)	15 × 4μs=60μs (16.7kHz)
01	Fosc/4	1MHz	250kHz (4μs)	15 × 4μs=60μs (16.7kHz)
10	Fosc/64	16MHz	250kHz (4μs)	15 × 4μs=60μs (16.7kHz)
11	Internal RC	-	14kHz (71μs)	15 × 71μs=1065μs (0.938kHz)

NOTE

- *Pin not used as an analog input pin can be used as regular input or output pin.*
- *During conversion, do not perform output instruction to maintain precision for all the pins.*

6.9.5 ADC Operation during Sleep Mode

In order to obtain a more accurate ADC value and reduce power consumption, the AD conversion remains operational during sleep mode. As the SLEP instruction is executed, all the MCU operations will stop except for the Oscillator, TCC, Timer 1, Timer 2, Timer 3, Timer 4 and AD conversion.

The AD Conversion is considered completed as determined by**:**

1. ADRUN bit of R9 register is cleared (“0” value)
2. Wake-up from AD conversion (where it remains in operation during sleep mode)

The results are fed into the ADDATA, ADDATA1H, and ADDATA1L registers when the conversion is completed. If the ADWE is enabled, the device will wake up. Otherwise, the AD conversion will be shut off, no matter what the status of ADPD bit is.

6.9.6 Programming Process/Considerations

6.9.6.1 Programming Process

Follow these steps to obtain data from the ADC:

1. Write to the 8 bits (ADE7:ADE0) on the Bank 2 R8 (AISR) register to define the characteristics of R6 (digital I/O, analog channels, or voltage reference pin).
2. Write to the Bank 2 R9/ADCON register to configure the AD module**:**
   a) Select ADC input channel (ADIS2: ADIS0).
   b) Define AD conversion clock rate (CKR1: CKR0).
   c) Select the VREFS input source of the ADC.
   d) Set the ADPD bit to 1 to begin sampling.
3. Set the ADWE bit, if the wake-up function is employed.
4. Set the ADIE bit, if the interrupt function is employed.
5. Write “ENI” instruction, if the interrupt function is employed.

6. Set the ADRUN bit to 1.
7. Write “SLEP” instruction or Polling.
8. Wait for wake-up or for ADRUN bit to be cleared (“0” value).
9. Read the ADDATA or ADDATA1H and ADDATA1L conversion data registers. If ADC input channel changes at this time, the ADDATA, ADDATA1H, and ADDATA1L values can be cleared to ‘0’.
10. Clear the interrupt flag bit (ADIF).
11. For next conversion, go to Step 1 or Step 2 as required. At least 2 Tct is required before the next acquisition starts.

NOTE

In order to obtain accurate values, it is necessary to avoid any data transition on I/O pins during AD conversion.

6.9.6.2 Sample Demo Programs

A. Define a General Registers

```
R_0 == 0          ; Indirect addressing register
PSW == 3          ; Status register
PORT5 == 5
PORT6 == 6
RE== 0XE          ; Wake-up control resister
RF== 0XF          ; Interrupt status register
```

B. Define a Control Register

```
IOC50 == 0X5      ; Control Register of Port 5
IOC60 == 0X6      ; Control Register of Port 6
C_INT== 0XF       ; Interrupt Control Register
```

C. ADC Control Register

```
ADDATA == 0xB     ; The contents are the results of ADC
AISR == 0x08      ; ADC Input select register
ADCON == 0x9      ;  7     6    5    4      3     2     1     0
                  ; VREFS CKR1 CKR0 ADRUN ADPD ADIS2 ADIS1 ADIS0
```

D. Define Bits in ADCON

```
ADRUN == 0x4      ; ADC is executed as the bit is set
ADPD == 0x3       ; Power Mode of ADC
```

E. Program Starts

```
ORG 0             ; Initial address
JMP INITIAL       ;

ORG 0x08          ; Interrupt vector
;
;
```

```
;(User program section)
;
;
CLR RF              ; To clear the ADIF bit
BS ADCON, ADRUN     ; To start to execute the next AD conversion
                    ; if necessary
RETI
INITIAL:
Bank 1
MOV A,@0B00000001   ; To define P60 as an analog input
MOV AISR,A
MOV A,@0B00001000   ; To select P60 as an analog input channel, and
                      AD power on
MOV ADCON,A         ; To define P60 as an input pin and set clock
                    ; rate at fosc/16
En_ADC:
MOV A, @0BXXXXXXX1  ; To define P50 as an input pin, and the others
IOW PORT6           ; are dependent on applications
MOV A, @0BXXXX1XXX  ; Enable the ADWE wake-up function of ADC, "X"
                    ; by application
MOV RE,A
MOV A, @0BXXXX1XXX  ; Enable the ADIE interrupt function of ADC,
                    ; "X" by application
IOW C_INT
ENI                 ; Enable the interrupt function

BS ADCON, ADRUN     ; Start to run the ADC

; If the interrupt function is employed, the following three lines
may be ignored

POLLING:
JBC ADCON, ADRUN    ; To check the ADRUN bit continuously;
JMP POLLING         ; ADRUN bit will be reset as the AD conversion
                    ; is completed
;
;
;(User program section)
;
;
```

6.10 Dual Sets of PWM (Pulse Width Modulation)

6.10.1 Overview

In PWM mode, PWM1, PWM2, and PWM3 pins generate a 10-bit resolution PWM output (see. the functional block diagram below). A PWM output consists of a time period and a duty cycle, and it keeps the output high. The baud rate of the PWM is the inverse of the time period. Fig. 6 -11 (*PWM Output Timing*) depicts the relationship between a time period and a duty cycle.

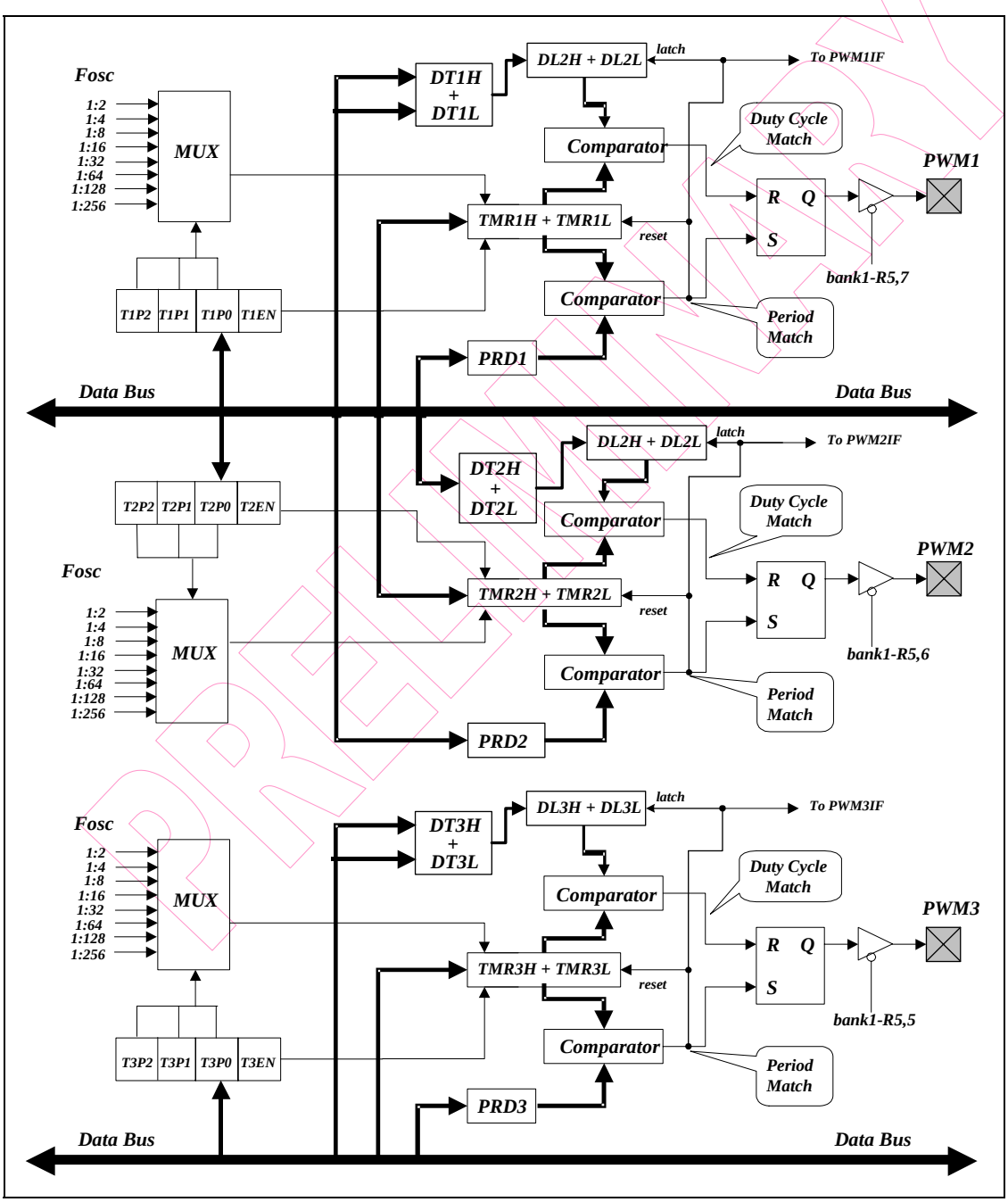


Fig. 6-10 The Three PWMs Functional Block Diagram

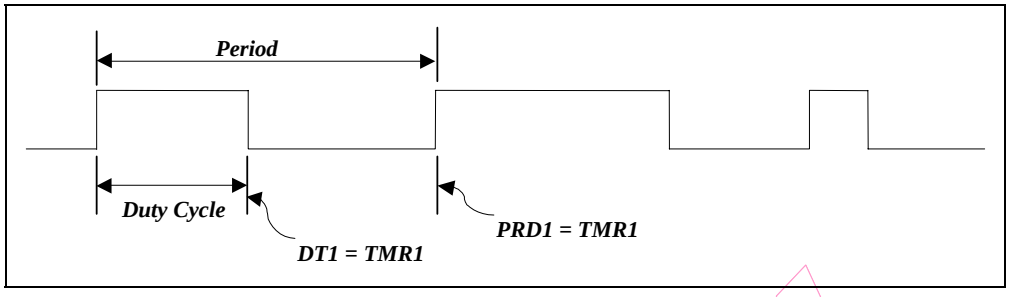


Fig. 6-11 PWM Output Timing

6.10.2 Increment Timer Counter (TMRX: TMR1H/TWR1L, TMR2H /TWR2L, or TMR3H/TWR3L)

TMRX are 10-bit clock counters with programmable prescalers. They are designed for the PWM module as baud rate clock generators. TMRX can be read only. If employed, they can be turned off for power saving by setting the T1EN bit [Bank 1 R5 <3>], T2EN bit [Bank 1 R6 <7>] or T3EN bit [Bank 1 R6 <3>] to 0.

6.10.3 PWM Time Period (PRDX : PRD1 or PRD2)

The PWM time period is defined by writing to the PRDX register. When TMRX is equal to PRDX, the following events occur on the next increment cycle:

- TMRX is cleared
- The PWMX pin is set to 1
- The PWM duty cycle is latched from DT1/DT2/DT3 to DL1/DL2/DL3

NOTE

The PWM output will not be set, if the duty cycle is 0.

- The PWMXIF pin is set to 1

The following formula describes how to calculate the PWM time period:

PERIOD = (PRDX + 1) * (1/Fosc) * CLKS/2 * (TMRX prescale value)

Example:

PRDX=49; Fosc=4MHz; CLKS bit of Code Option Register =0 (2 oscillator periods); TMRX (0, 0, 0) = 1:2, then PERIOD=(49 + 1) * (1/4M) * 2/2 * 2 = 25us

6.10.4 PWM Duty Cycle(DTX: DT1H/ DT1L, DT2H/ DT2L and DT3H/DT3L; DLX: DL1H/DL1L, DL2H/DL2L and DL3H/DL3L)

The PWM duty cycle is defined by writing to the DTX register, and is latched from DTX to DLX while TMRX is cleared. When DLX is equal to TMRX, the PWMX pin is cleared. DTX can be loaded anytime. However, it cannot be latched into DLX until the current value of DLX is equal to TMRX.

The following formula describes how to calculate the PWM duty cycle:

Duty Cycle = (DTX) * (1/Fosc) * CLKS/2 * (TMRX prescale value)

Example:

DTX=10; Fosc=4MHz; CLKS bit of Code Option Register = 0 (2 oscillator periods); TMRX (0,0,0)=1:2, then Duty Cycle = 10 * (1/4M) * 2/2 * 2 =5us

6.10.5 Comparator X

Changing the output status while a match occurs will simultaneously set the TMRXIF flag.

6.10.6 PWM Programming Process/Steps

1. Load PRDX with the PWM time period.
2. Load DTX with the PWM Duty Cycle.
3. Enable interrupt function by writing IOCF, if required.
4. Set PWMX pin to be output by writing a desired value to Bank1 R5 or R6.
5. Load a desired value to Bank1 R5 or R6 with TMRX prescaler value and enable both PWMX and TMRX.

6.11 Timer

6.11.1 Overview

Timer 1 (TMR1), Timer 2 (TMR2), and Timer 3 (TMR3) (TMRX) are 10-bit clock counters with programmable prescalers. They are designed for the PWM module as baud rate clock generators. TMRX can be read only. The Timer 1, Timer 2, and Timer 3 will stop running when sleep mode occurs with AD conversion not running. However, if AD conversion is running when sleep mode occurs, the Timer 1, Timer 2 and Timer 3, will keep on running.

6.11.2 Function Description

The following figure shows the TMRX block diagram followed by descriptions of its signals and blocks:

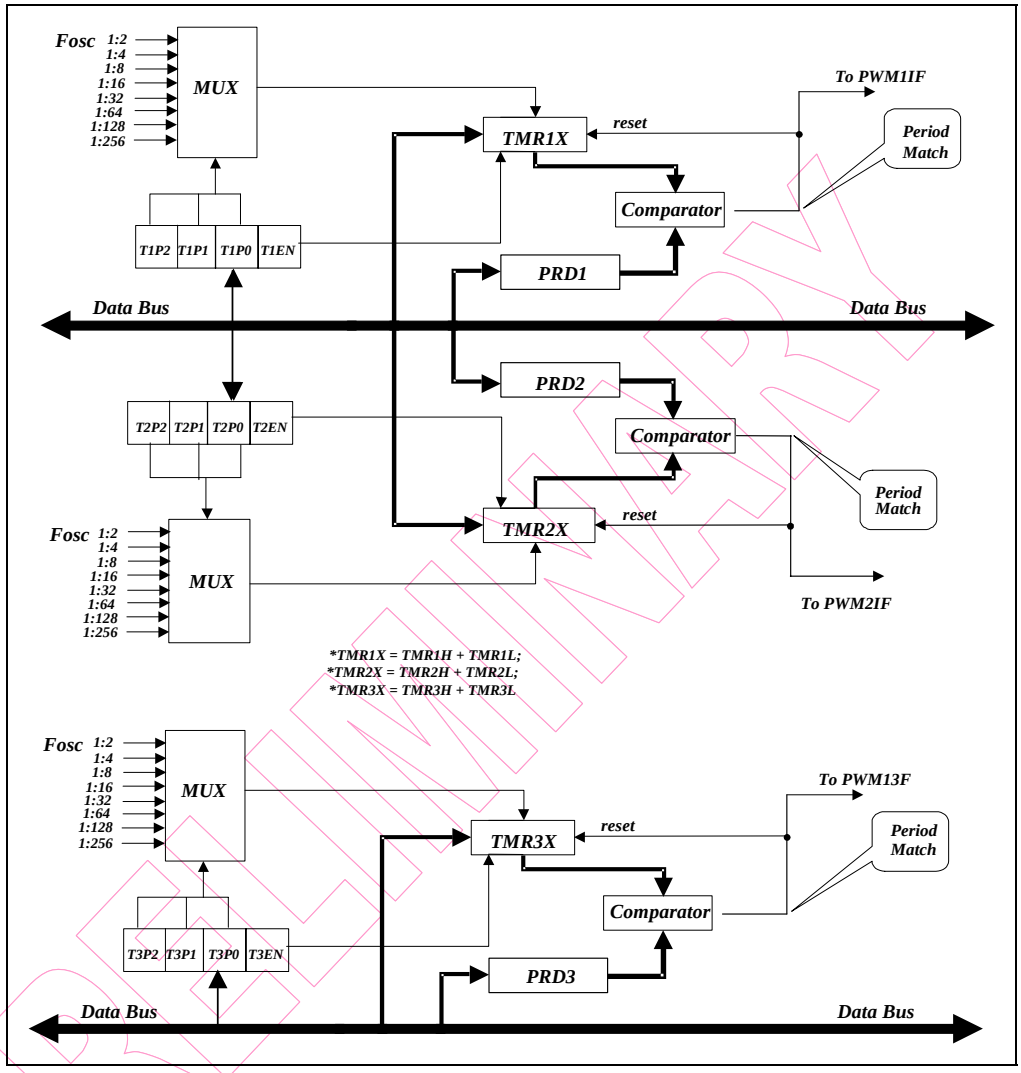


Fig. 6-12 TMRX Block Diagram

Fosc: Input clock.

Prescaler (T1P2, T1P1 and T1P0 / T2P2, T2P1 and T2P0 / T3P2, T3P1 and T3P0):
The options 1:2, 1:4, 1:8, 1:16, 1:32, 1:64, 1:128, and 1:256 are defined by TMRX. It is cleared when any type of reset occurs.

TMR1X, TMR2X and TMR3X (TMR1H/TWR1L, TMR2H/TMR2L, & TMR3H/TMR3L):
Timer X register; TMRX is incremented until it matches with PRDX, and then is reset to 1 (default valve).

PRDX (PRD1/PRD1H, PRD2/PRD2H and PRD3/PRD3H):
PWM time period register.

ComparatorX (Comparator 1 and Comparator 2):
Reset TMRX while a match occurs. The TMRXIF flag is set at the same time.

6.11.3 Programming the Related Registers

When defining TMRX, refer to the related registers of its operation as shown in the table below. It must be noted that the PWMX bits must be disabled if their related TMRXs are employed. That is, Bit 7 ~ Bit 5 of the PWMCON register must be set to '0'.

6.11.3.1 Related Control Registers of TMR1, TMR2, and TMR3

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x05	PWMCON#1/Bank1 R5	PWM3E	PWM2E	PWM1E	"0"	T1EN	T1P2	T1P1	T1P0
0x06	PWMCON#2/Bank1 R6	T2EN	T2P2	T2P1	T2P0	T3EN	T3P2	T3P1	T3P0

6.11.4 Timer Programming Process/Steps

1. Load PRDX with the TIMER duration
2. Enable interrupt function by writing IOCF, if required
3. Load a desired a TMRX prescaler value to PWMCON and TMRCON and enable TMRX and disable PWMX

6.12 Comparator

EM78P350N has one comparator comprising of two analog inputs and one output. The comparator can be utilized to wake up the EM78P350N from sleep mode. The comparator circuit diagram is depicted in the figure below.

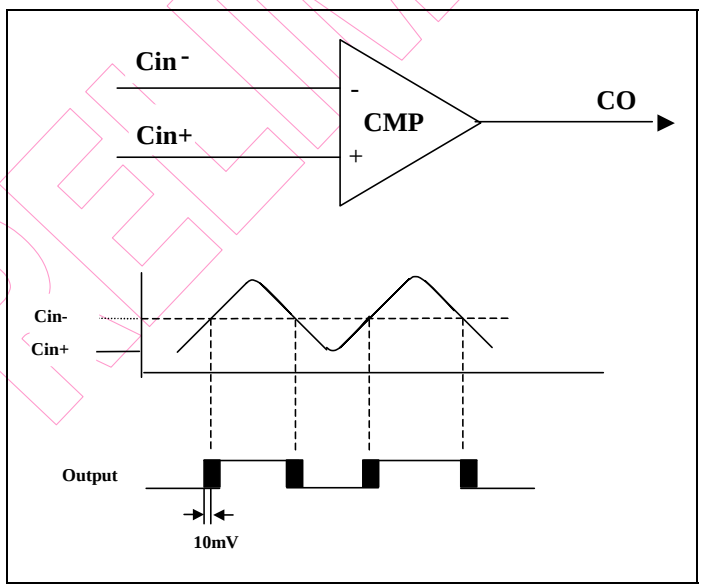


Fig. 6-13 Comparator Circuit Diagram & Operating Mode

6.12.1 External Reference Signal

The analog signal that is presented at Cin– compares to the signal at Cin+, and the digital output (CO) of the comparator is adjusted accordingly by taking the following notes into considerations:

NOTE

- *The reference signal must be between Vss and Vdd.*
- *The reference voltage can be applied to either pin of the comparator.*
- *Threshold detector applications may be of the same reference.*
- *The comparator can operate from the same or different reference sources.*

6.12.2 Comparator Outputs

- The compared result is stored in the CMPOUT of IOCA0.
- The comparator outputs are sent to CO (P56) through programming Bit 1, Bit 0<COS1, COS0> of the IOCA0 register to <1, 0>. See Section 6.2.7, *IOCA0 (CMPCON: Comparator Control Register)* for Comparator/OP select bits function description.

NOTE

- *The P56/CO pin priority is as follows:*

P60/ADE0/CO Priority	
High	Low
CO	P56

The following figure shows the Comparator Output block diagram.

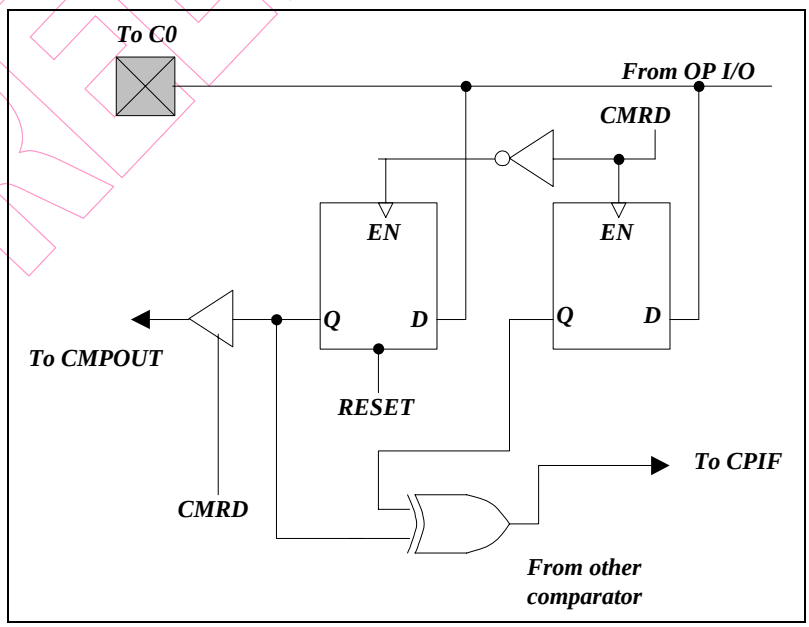


Fig. 6-14 Comparator Output Configuration

6.12.3 Using Comparator as an Operation Amplifier

The comparator can be used as an operation amplifier if a feedback resistor is connected from the input to the output externally. In this case, the Schmitt Trigger can be disabled for power saving by setting Bit 1, Bit 0<COS1, COS0> of the IOCA0 register to <1, 1>. See Section 6.2.6, *IOCA0 (CMPCON: Comparator Control Register)* for Comparator/OP select bits function description.

6.12.4 Comparator Interrupt

- CMPIE (IOCE.0) must be enabled for the "ENI" instruction to take effect.
- Interrupt is triggered whenever a change occurs on the comparator output pin.
- The actual change on the pin can be determined by reading the Bit CMPOUT, IOCA0 < 2 >.
- CMPIF (RE.0), the comparator interrupt flag, can only be cleared by software.

6.12.5 Wake-up from Sleep Mode

- If enabled, the comparator remains active and the interrupt remains functional, even in Sleep mode.
- If a mismatch occurs, the interrupt will wake up the device from Sleep mode.
- The power consumption should be taken into consideration for the benefit of energy conservation.
- If the function is unemployed during Sleep mode, turn off the comparator before entering into Sleep mode.

6.13 Oscillator

6.13.1 Oscillator Modes

The EM78P350N can be operated in four different oscillator modes namely, High Crystal oscillator mode (HXT), Low Crystal oscillator mode (LXT), External RC oscillator mode (ERC), and RC oscillator mode with Internal RC oscillator mode (IRC). One of such modes can be selected by programming the OSC2, OCS1, and OSC0 in the Code Option register.

The Oscillator modes defined by OSC2, OCS1, and OSC0 are described below.

Oscillator Modes	OSC2	OSC1	OSC0
ERC[1] (External RC oscillator mode); P50/OSCO acts as P50	0	0	0
ERC[1] (External RC oscillator mode); P50/OSCO acts as OSCO	0	0	1
IRC[2] (Internal RC oscillator mode); P50/OSCO acts as P50	0	1	0
IRC[2] (Internal RC oscillator mode); P50/OSCO acts as OSCO	0	1	1
LXT[3] (Low Crystal oscillator mode)	1	1	0
HXT[3] High Crystal oscillator mode) (default)	1	1	1

[1] In ERC mode, OSCI is used as oscillator pin. OSCO/P50 is defined by code option Word 0 Bit 6 ~ Bit 4.

[2] In IRC mode, P55 is normal I/O pin. OSCO/P50 is defined by code option Word 0 Bit 6 ~ Bit 4.

[3] In LXT and HXT modes; OSCI and OSCO are used as oscillator pins. These pins cannot and should not be defined as normal I/O pins.

NOTE

The transient point of the system frequency between HXT and LXY is 400kHz.

The maximum operating frequency limit of crystal/resonator at different VDDs, are as follows:

Conditions	VDD	Max. Freq. (MHz)
Two clocks	2.3	4
	3.0	8
	5.0	20

6.13.2 Crystal Oscillator/Ceramic Resonators (Crystal)

The EM78P350N can be driven by an external clock signal through the OSCI pin as illustrated below.

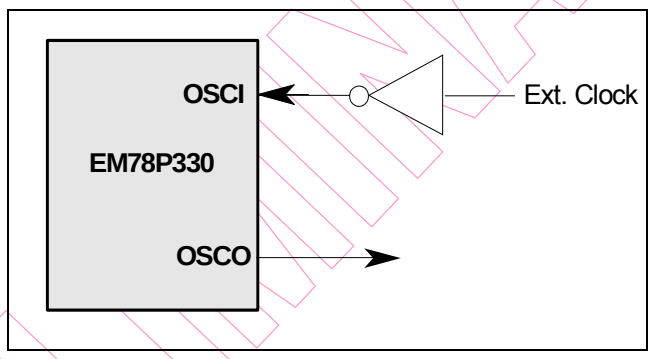


Fig. 6.15 External Clock Input Circuit

In the most applications, Pin OSCI and Pin OSCO can be connected with a crystal or ceramic resonator to generate oscillation. Fig. 6-16 below depicts such a circuit. The same applies to the HXT mode and the LXT mode.

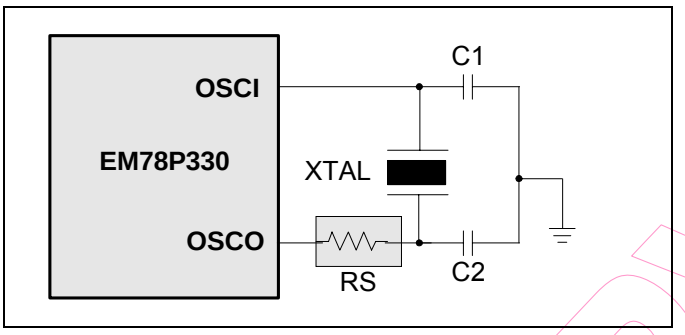


Fig. 6-16 Crystal/Resonator Circuit

The following table provides the recommended values for C1 and C2. Since each resonator has its own attribute, user should refer to the resonator specifications for appropriate values of C1 and C2. RS, a serial resistor, may be required for AT strip cut crystal or low frequency mode.

Capacitor selection guide for crystal oscillator or ceramic resonators:

Oscillator Type	Frequency Mode	Frequency	C1 (pF)	C2 (pF)
Ceramic Resonators	HXT	455 kHz	100~150	100~150
		2.0 MHz	20~40	20~40
		4.0 MHz	10~30	10~30
Crystal Oscillator	LXT	32.768 kHz	25	15
		100 kHz	25	25
		200 kHz	25	25
	HXT	455 kHz	20~40	20~150
		1.0 MHz	15~30	15~30
		2.0 MHz	15	15
		4.0 MHz	15	15

6.13.3 External RC Oscillator Mode

For some applications that do not require precise timing calculation, the RC oscillator (Fig. 6-17 at right) offers a cost-effective solution. Nevertheless, it should be noted that the frequency of the RC oscillator is influenced by the supply voltage, the values of the resistor (Rext), the capacitor (Cext), and even by the operation temperature. Moreover, the frequency also changes slightly from one chip to another due to manufacturing process variations.

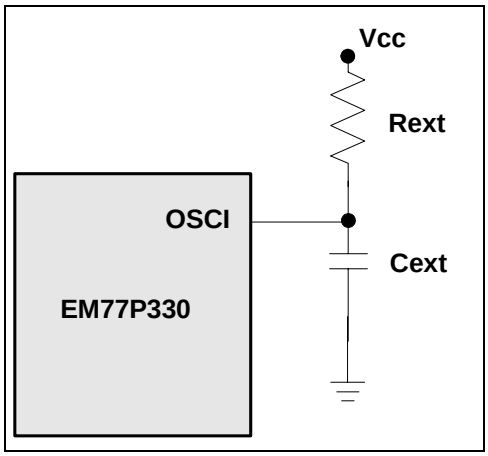


Fig. 6-17 External RC Oscillator Mode Circuit

In order to maintain a stable system frequency, the values of the Cext should be no less than 20pF, and the value of Rext should be no greater than 1MΩ. If the frequency cannot be kept within this range, the frequency can be affected easily by noise, humidity, and leakage.

The smaller the Rext in the RC oscillator is, the faster its frequency will be. On the contrary, for very low Rext values, for instance, 1 KΩ, the oscillator will become unstable because the NMOS cannot correctly discharge the capacitance current.

Based on the above reasons, it must be kept in mind that all supply voltage, the operation temperature, the components of the RC oscillator, the package types, and the way the PCB is layout, have certain effects on the system frequency.

The RC Oscillator frequencies**:**

Cext	Rext	Average Fosc 5V, 25°C	Average Fosc 3V, 25°C
20 pF	3.3k	3.5 MHz	3.2 MHz
	5.1k	2.5 MHz	2.3 MHz
	10k	1.30 MHz	1.25 MHz
	100k	140 kHz	140 KHz
100 pF	3.3k	1.27 MHz	1.21 MHz
	5.1k	850 kHz	820 kHz
	10k	450 kHz	450 kHz
	100k	48 kHz	50 kHz
300 pF	3.3k	560 kHz	540 kHz
	5.1k	370 kHz	360 kHz
	10k	196 kHz	192 kHz
	100k	20 kHz	20 kHz

Note: [1]: Measured based on DIP packages.

[2]: The values are for design reference only.

[3]: The frequency drift is ± 30%

6.13.4 Internal RC Oscillator Mode

The EM78P350N offers a versatile internal RC mode with default frequency value of 4MHz. Internal RC oscillator mode has other frequencies (1 MHz, 8 MHz, and 455 kHz) that can be set by Code Option (Word 1), RCM1, and RCM0. The Table below describes the EM78P350N internal RC drift with voltage, temperature, and process variations.

Internal RC Drift Rate (Ta=25°C, VDD=5V±5%, VSS=0V)

Internal RC Frequency	Drift Rate			
	Temperature (-40°C~+85°C)	Voltage (2.3V~5.5V)	Process	Total
4MHz	±10%	±5%	±4%	±19%
8MHz	±10%	±6%	±4%	±20%
1MHz	±10%	±5%	±4%	±19%
455MHz	±10%	±5%	±4%	±19%

Theoretical values are for reference only. Actual values may vary depending on the actual process.

6.14 Power-on Considerations

Any microcontroller is not warranted to start operating properly before the power supply stabilizes to a steady state. The EM78P350N has a built-in Power-on Voltage Detector (POVD) with detection level range of 1.9V to 2.1V. The circuitry eliminates the extra external reset circuit. It will work well if Vdd rises quickly enough (50 ms or less). However, under critical applications, extra devices are still required to assist in solving power-on problems.

6.14.1 External Power-on Reset Circuit

The circuits shown in the following figure implements an external RC to produce a reset pulse. The pulse width (time constant) should be kept long enough to allow Vdd to reach the minimum operating voltage. This circuit is used when the power supply has a slow power rise time. Because the current leakage from the /RESET pin is about ±5μA, it is recommended that R should not be greater than 40 K. This way, the voltage at Pin /RESET is held below 0.2V. The diode (D) functions as a short circuit at power-down. The “C” capacitor is discharged rapidly and fully. Rin, the current-limited resistor, prevents high current discharge or ESD (electrostatic discharge) from flowing into Pin /RESET.

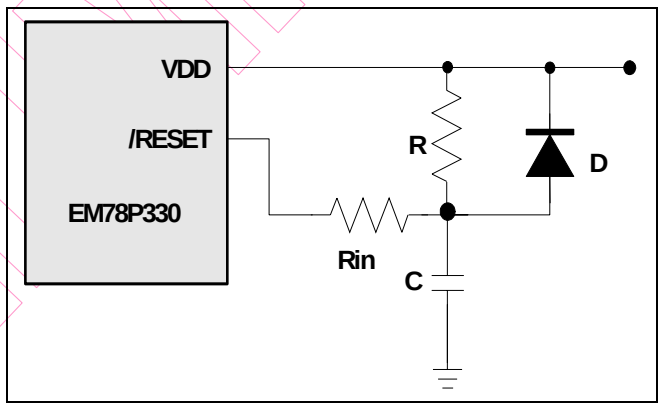


Fig. 6-18 External Power on Reset Circuit

6.14.2 Residual Voltage Protection

When the battery is replaced, device power (Vdd) is removed but residual voltage remains. The residual voltage may trip below Vdd minimum, but not to zero. This condition may cause a poor power-on reset. Fig. 6-16 and Fig. 6-20 show how to create a protection circuit against residual voltage.

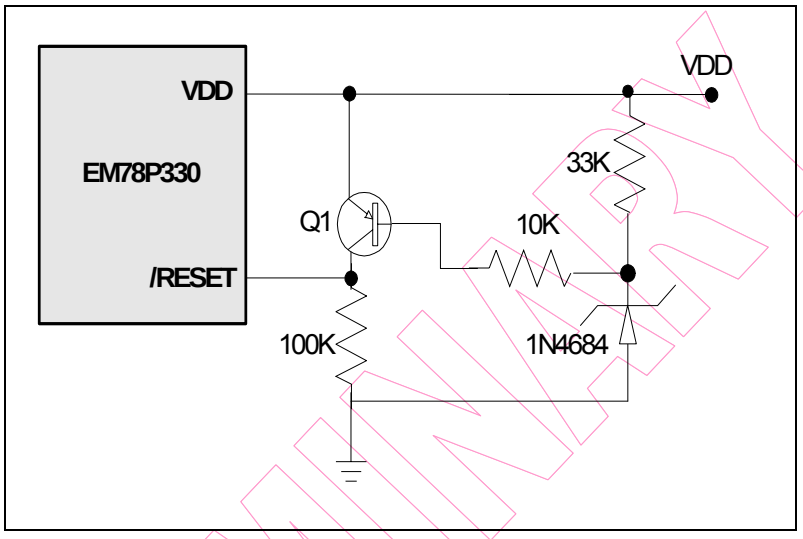


Fig. 6-19 Residual Voltage Protection Circuit 1

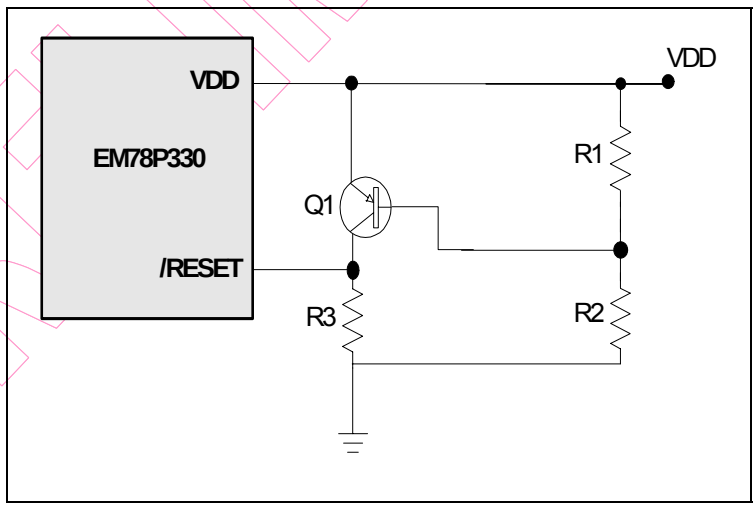


Fig. 6-20 Residual Voltage Protection Circuit 2

6.15 LVD (Low Voltage Detector)

During the power source unstable situation, such like external power noise interference of EMS test condition, it will cause the power vibrate fierce. At the time the Vdd is unsettled, it may be below working voltage. When system supplies voltage, Vdd, below the working voltage, the IC kernel must keep all register status automatically. LVD property is setting at Register RE, Bit 1, 0 detail operation mode as follows:

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
"0"	"0"	"0"	"0"	LVDEN	/LVD	LVD1	LVD0

Bits 1 ~ 0 (LVD1 ~ LVD0): Low Voltage Detect level control Bits.

LVDEN <RA, 2>	LVD1,LVD0 <RA, 1, 0>	LVD Voltage Interrupt Level	LVDIF
1	11	2.2V	1*
1	10	3.3V	1*
1	01	4.0V	1*
1	00	4.5V	1*
0	XX	NA	0

* If Vdd has crossover at LVD voltage interrupt level as Vdd changes, LVDIF =1.

The LVD status and interrupt flag is referred to as RF

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RF	"0"	"0"	"0"	LVDIF	ADWE	CMPWE	ICWE	PWMWE

Note: "1" means with interrupt request
"0" means no interrupt occurs

Bit 4 (LVDIF): Low Voltage Detector Interrupt Register

The following steps are needed to setup the LVD function:

Set the LVDEN of Register RE of Bank 2 to"1", then use Bit 1, 0 (LVD1, LVD0) of Register RE of Bank 2 to set the LVD interrupt level while waiting for an interrupt to occur.

The internal LVD module is using internal circuit to fit. When you set the LVDEN enable the LVD module. The current consumption will increase about 10μA. During sleep mode, the LVD module continues to operate. If the device voltage drops slowly and crosses the detect point, the LVDIF bit will be set and device won't wake up from sleep time. Until the other wake-up source of EM78P350N, the LVD interrupt flag still set as the prior status.

When the system resets, the LVD flag will be cleared.

When Vdd drops not below VLVD, LVDIF remains at "0".

When Vdd drops below VLVD, LVDIF is set to "1". If in global ENI enable, LVDIF will be set to "1", the next instruction will branch to an interrupt vector. The LVD interrupt flag is cleared to "0" by software.

When Vdd drops below VRESET to less than 80μs, the system will ignore it and keep going. When Vdd drops below VRESET to more than 80μs, a system reset will occur. Refer to Section 6.5.1 for Reset description.

6.16 Code Option

The EM78P350N has two Code option words and one Customer ID word that are not part of the normal program memory.

Word 0	Word 1	Word 2
Bit 12 ~ Bit 0	Bit 12 ~ Bit 0	Bit 12 ~ Bit 0

6.16.1 Code Option Register (Word 0)

Word 0												
Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
-	LVR1	LVR0	LCE	CLKS	ENWDTB	OSC2	OSC1	OSC0	HLP	PR2	PR1	PR0

Bit 12: Unimplemented, read as "0".

Bits 11 ~ 10: Low voltage reset enable bits.

LVR1, LVR0	Reset Level	Release Level
00	4.0V	4.2V
01	3.5V	3.7V
10	2.7V	2.9V
11	NA	NA

If VDD < 1.8V, the IC will be reset.

If VDD < 2.7V, the IC will be reset.

If VDD < 3.5V, the IC will be reset.

If VDD < 4.0V, the IC will be reset.

Bit 9 (LCE): Low crystal output enable

1 : Select General-purpose I/O (P74, P73)

0 : Low crystal 32.768kHz mode. P74, P73 can be connected to a low crystal.

Bit 8 (CLKS): Instruction time period option bit

0 = two oscillator time periods

1 = four oscillator time periods (default)

Refer to the Section 6.15 for Instruction Set

Bit 7 (ENWDTB): Watchdog timer enable bit

0 = Enable

1 = Disable (default)

Bits 6, 5 & 4 (OSC2, OSC1 & OSC0): Oscillator Modes Selection bits

Oscillator Modes	OSC2	OSC1	OSC0
ERC[1] (External RC oscillator mode); P50/OSCO functions as P50	0	0	0
ERC[1] (External RC oscillator mode); P50/OSCO functions as OSCO	0	0	1
IRC[2] (Internal RC oscillator mode); P50/OSCO functions as P50	0	1	0
IRC[2] (Internal RC oscillator mode); P50/OSCO functions as OSCO	0	1	1
LXT[3] (Low Crystal oscillator mode)	1	1	0
HXT[3] (High Crystal oscillator mode) (default)	1	1	1

[1] In ERC mode, OSCI is used as oscillator pin. OSCO/P50 is defined by code option Word 0 Bit 6 ~ Bit 4.

[2] In IRC mode, P51 is normal I/O pin. OSCO/P50 is defined by code option Word 0 Bit 6 ~ Bit 4.

[3] In LXT and HXT modes; OSCI and OSCO are used as oscillator pins. These pins cannot and should not be defined as normal I/O pins.

NOTE

The transient point of the system frequency between HXT and LXY is 400kHz.

Bit 3 (HLP): Power consumption selection

0 = Low power consumption, applies to working frequency at 4MHz or below 4MHz

1 = High power consumption, applies to working frequency above 4MHz

Bits 2 ~ 0 (PR2 ~ PR0): Protect Bit

PR2 ~ PR0 are protection bits. Each protect status is as follows:

PR2	PR1	PR0	Protect
0	0	0	Enable
0	0	1	Enable
0	1	0	Enable
0	1	1	Enable
1	0	0	Enable
1	0	1	Enable
1	1	0	Enable
1	1	1	Disable

6.16.2 Code Option Register (Word 1)

Word 1												
Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
–	–	–	POREN	NRHL	NRE	CYES	C3	C2	C1	C0	RCM1	RCM0

Bits 12~10: Not used, (reserved). These bits are set to "1" all the time.

Bit 9 (POREN): Power on Reset Enable/Disable bit

0 = Disable power-on reset

1 = Enable power-on reset (default)

Bit 8 (NRHL): Noise rejection high/low pulses define bit when the signal at INT pin has a falling edge trigger.

0 = Pulses equal to 8/fc is regarded as signal

1 = Pulses equal to 32/fc is regarded as signal (default)

NOTE

The noise rejection function is turned off under the LXT and sleep mode.

Bit 7 (NRE): Noise rejection enable

0 = disable noise rejection

1 = enable noise rejection (default). However in Low Crystal oscillator (LXT) mode, the noise rejection circuit is always disabled.

Bit 6 (CYES): Instruction cycle selection bit

0 = one instruction cycle

1 = two instruction cycles (default)

Bits 5, 4, 3 & Bit 2 (C3, C2, C1, & C0): Internal RC mode Calibration bits. These bits must always be set to "1" only (auto calibration)

Bit 1 & Bit 0 (RCM1 & RCM0): RC mode selection bits

RCM 1	RCM 0	Frequency (MHz)
1	1	4
1	0	8
0	1	1
0	0	455kHz

6.15.3 Customer ID Register (Word 2)

Word 2												
Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
×	×	×	×	×	×	×	×	×	×	×	×	×

Bits 12 ~ 0 : Customer's ID code

6.17 Instruction Set

Each instruction in the instruction set is a 13-bit word divided into an OP code and one or more operands. Normally, all instructions are executed within one single instruction cycle (one instruction consists of 2 oscillator time periods), unless the program counter is changed by instructions "MOV R2,A," "ADD R2,A," or by instructions of arithmetic or logic operation on R2 (e.g., "SUB R2,A," "BS(C) R2,6," "CLR R2," etc.). In this case, these instructions need one or two instruction cycles as determined by Code Option Register CYES bit.

In addition, the instruction set has the following features:

1. Every bit of any register can be set, cleared, or tested directly.
2. The I/O registers can be regarded as general registers. That is, the same instruction can operate on I/O registers.

Convention:

R = Register designator that specifies which one of the registers (including operation and general purpose registers) is to be utilized by the instruction.

b = Bit field designator that selects the value for the bit located in the register R and which affects the operation.

k = 8 or 10-bit constant or literal value

Binary Instruction	HEX	Mnemonic	Operation	Status Affected
0 0000 0000 0000	0000	NOP	No Operation	None
0 0000 0000 0001	0001	DAA	Decimal Adjust A	C
0 0000 0000 0010	0002	CONTW	A → CONT	None
0 0000 0000 0011	0003	SLEP	0 → WDT, Stop oscillator	T, P
0 0000 0000 0100	0004	WDTC	0 → WDT	T, P
0 0000 0000 rrrr	000r	IOW R	A → IOCR	None[1]
0 0000 0001 0000	0010	ENI	Enable Interrupt	None
0 0000 0001 0001	0011	DISI	Disable Interrupt	None
0 0000 0001 0010	0012	RET	[Top of Stack] → PC	None
0 0000 0001 0011	0013	RETI	[Top of Stack] → PC, Enable Interrupt	None
0 0000 0001 0100	0014	CONTR	CONT → A	None
0 0000 0001 rrrr	001r	IOR R	IOCR → A	None[1]
0 0000 01rr rrrr	00rr	MOV R,A	A → R	None
0 0000 1000 0000	0080	CLRA	0 → A	Z
0 0000 11rr rrrr	00rr	CLR R	0 → R	Z
0 0001 00rr rrrr	01rr	SUB A,R	R-A → A	Z,C, DC
0 0001 01rr rrrr	01rr	SUB R,A	R-A → R	Z,C, DC
0 0001 10rr rrrr	01rr	DECA R	R-1 → A	Z
0 0001 11rr rrrr	01rr	DEC R	R-1 → R	Z

Binary Instruction	HEX	Mnemonic	Operation	Status Affected
0 0010 00rr rrrr	02rr	OR A,R	A ∨ VR → A	Z
0 0010 01rr rrrr	02rr	OR R,A	A ∨ VR → R	Z
0 0010 10rr rrrr	02rr	AND A,R	A & R → A	Z
0 0010 11rr rrrr	02rr	AND R,A	A & R → R	Z
0 0011 00rr rrrr	03rr	XOR A,R	A ⊕ R → A	Z
0 0011 01rr rrrr	03rr	XOR R,A	A ⊕ R → R	Z
0 0011 10rr rrrr	03rr	ADD A,R	A + R → A	Z, C, DC
0 0011 11rr rrrr	03rr	ADD R,A	A + R → R	Z, C, DC
0 0100 00rr rrrr	04rr	MOV A,R	R → A	Z
0 0100 01rr rrrr	04rr	MOV R,R	R → R	Z
0 0100 10rr rrrr	04rr	COMA R	/R → A	Z
0 0100 11rr rrrr	04rr	COM R	/R → R	Z
0 0101 00rr rrrr	05rr	INCA R	R+1 → A	Z
0 0101 01rr rrrr	05rr	INC R	R+1 → R	Z
0 0101 10rr rrrr	05rr	DJZA R	R-1 → A, skip if zero	None
0 0101 11rr rrrr	05rr	DJZ R	R-1 → R, skip if zero	None
0 0110 00rr rrrr	06rr	RRCA R	R(n) → A(n-1), R(0) → C, C → A(7)	C
0 0110 01rr rrrr	06rr	RRC R	R(n) → R(n-1), R(0) → C, C → R(7)	C
0 0110 10rr rrrr	06rr	RLCA R	R(n) → A(n+1), R(7) → C, C → A(0)	C
0 0110 11rr rrrr	06rr	RLC R	R(n) → R(n+1), R(7) → C, C → R(0)	C
0 0111 00rr rrrr	07rr	SWAPA R	R(0-3) → A(4-7), R(4-7) → A(0-3)	None
0 0111 01rr rrrr	07rr	SWAP R	R(0-3) ↔ R(4-7)	None
0 0111 10rr rrrr	07rr	JZA R	R+1 → A, skip if zero	None
0 0111 11rr rrrr	07rr	JZ R	R+1 → R, skip if zero	None
0 100b bbrr rrrr	0xxx	BC R,b	0 → R(b)	None[1]
0 101b bbrr rrrr	0xxx	BS R,b	1 → R(b)	None[2]
0 110b bbrr rrrr	0xxx	JBC R,b	if R(b)=0, skip	None
0 111b bbrr rrrr	0xxx	JBS R,b	if R(b)=1, skip	None
1 00kk kkkk kkkk	1kkk	CALL k	PC+1 → SP, (Page, k) → PC	None
1 01kk kkkk kkkk	1kkk	JMP k	(Page, k) → PC	None

Binary Instruction	HEX	Mnemonic	Operation	Status Affected
1 1000 kkkk kkkk	18kk	MOV A,k	k → A	None
1 1001 kkkk kkkk	19kk	OR A,k	A ∨ k → A	Z
1 1010 kkkk kkkk	1Akk	AND A,k	A & k → A	Z
1 1011 kkkk kkkk	1Bkk	XOR A,k	A ⊕ k → A	Z
1 1100 kkkk kkkk	1Ckk	RETL k	k → A, [Top of Stack] → PC	None
1 1101 kkkk kkkk	1Dkk	SUB A,k	k-A → A	Z,C,DC
1 1110 1000 kkkk	1E8k	PAGE k	k → R1(5:4)	None
1 1110 1001 kkkk	1E9k	BANK k	k → R1(1:0)	None
1 1111 kkkk kkkk	1Fkk	ADD A,k	k+A → A	Z, C, DC

Note: [1] This instruction is applicable to IOC50 ~ IOCF, IOC51 ~ IOCF1 only.

[2] This instruction is not recommended for RF operation

[3] This instruction cannot operate under RF.

7 Absolute Maximum Ratings

Items	Rating		
Temperature under bias	-40°C	to	85°C
Storage temperature	-65°C	to	150°C
Input voltage	Vss-0.3V	to	Vdd+0.5V
Output voltage	Vss-0.3V	to	Vdd+0.5V
Working Voltage	2.3V	to	5.5V
Working Frequency	DC	to	20MHz

8 DC Electrical Characteristics

Ta= 25 °C, VDD= 5.0V, VSS= 0V

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
FXT	Crystal: VDD to 5V	Two cycles with two clocks	DC		20	MHz
	Crystal: VDD to 3V		DC		8	MHz
	ERC: VDD to 5V	R: 5.1KΩ, C: 100 pF	F±30%	850	F±30%	kHz
IRC1	IRC:VDD to 5V	RCM0:RCM1=1:1	3.84	4.0	4.16	MHz
IRC2	IRC:VDD to 5V	RCM0:RCM1=1:0	7.68	8.0	8.32	MHz
IRC3	IRC:VDD to 5V	RCM0:RCM1=0:1	0.96	1.0	1.06	MHz
IRC4	IRC:VDD to 5V	RCM0:RCM1=0:0	436.8	455	473.2	kHz
VIHRC	Input High Threshold Voltage (Schmitt Trigger)	OSCI in RC mode	–	3.5	–	V
VILRC	Input Low Threshold Voltage (Schmitt Trigger)	OSCI in RC mode	–	1.5	–	V
IIL	Input Leakage Current for input pins	VIN = VDD, VSS	–1.0	0	1.0	µA
VIH1	Input High Voltage (Schmitt Trigger)	Ports 5, 6, 7, 8	–	3.75	–	V
VIL1	Input Low Voltage (Schmitt Trigger)	Ports 5, 6, 7, 8	–	1.25	–	V
VIHT1	Input High Threshold Voltage (Schmitt Trigger)	/RESET	–	2.0	–	V
VILT1	Input Low Threshold Voltage (Schmitt Trigger)	/RESET	–	1.0	–	V
VIHT2	Input High Threshold Voltage (Schmitt Trigger)	TCC,INT	–	3.75	–	V
VILT2	Input Low Threshold Voltage (Schmitt Trigger)	TCC,INT	–	1.25	–	V
VIHX1	Clock Input High Voltage	OSCI in crystal mode	–	3.5	–	V
VILX1	Clock Input Low Voltage	OSCI in crystal mode	–	1.5	–	V
IOH1	Output High Voltage (Ports 50~53, Ports 60~63) (Ports 70~77, Ports 80~84)	VOH = VDD-0.5V (IOH =-6mA)	–	-9.0	–	mA
IOH2	Output High Voltage (Ports P54~P57, P64~P67)	VOH = VDD-0.5V (IOH =-9mA)	–	-12.0	–	mA
IOL1	Output Low Voltage (Ports 50~53, Ports 60~63) (Ports 70~77, Ports 80~84)	VOL = GND+0.5V (IOL =12mA)	–	18.0	–	mA
IOL2	Output Low Voltage (Ports P54~P57, P64~P67)	VOL = GND+0.5V (IOL =24mA)	–	24.0	–	mA
IBOL	Output Sink Current	Buzzer output sink current	–	24	–	mA
IBOH	Output Drive Current	Buzzer output drive current	–	24	–	mA
IPH	Pull-high current	Pull-high active, input pin at VSS	–50	–75	–240	µA
IPL	Pull-low current	Pull-low active, input pin at Vdd	25	40	120	µA
ISB1	Power down current	All input and I/O pins at VDD, Output pin floating, WDT disabled	–	1.0	2.0	µA
ISB2	Power down current	All input and I/O pins at VDD, Output pin floating, WDT enabled	–	–	15	µA
ICC1	Operating supply current at two clocks	/RESET= 'High', Fosc=32kHz, (Crystal type, CLKS="0"), Output pin floating, WDT disabled	15	20	35	µA
ICC2	Operating supply current at two clocks	/RESET= 'High', Fosc=32kHz (Crystal type, CLKS="0"), Output pin floating, WDT enabled		25	35	µA
ICC3	Operating supply current at two clocks	/RESET= 'High', Fosc=4MHz (Crystal type, CLKS="0"), Output pin floating, WDT enabled		1.7	2.2	mA
ICC4	Operating supply current at two clocks	/RESET= 'High', Fosc=10MHz (Crystal type, CLKS="0"), Output pin floating, WDT enabled		3.0	3.5	mA

8.1 AD Converter Characteristic

Vdd=2.5V to 5.5V, Vss=0V, Ta=25°C

Symbol		Parameter	Condition	Min.	Typ.	Max.	Unit
V_{AREF}		Analog reference voltage	V_{AREF} - $V_{ASS} \geq$ 2.3V	2.3	–	Vdd	V
V_{ASS}				Vss	–	Vss	V
VAI		Analog input voltage	–	V_{ASS}	–	V_{AREF}	V
IAI1	Ivdd	Analog supply current	Vdd=V_{AREF}=5.0V, V_{ASS} =0.0V (V reference from Vdd)	750	850	1000	uA
	Ivref			-10	0	+10	uA
IAI2	Ivdd	Analog supply current	Vdd=V_{AREF}=5.0V, V_{ASS} =0.0V (V reference from VREF)	500	600	820	uA
	IVref			200	250	300	uA
IOP		OP current	Vdd=5.0V, OP used Output voltage swing 0.15V to 4.85V	450	550	650	uA
RN		Resolution	Vdd=V_{AREF}=5.0V, V_{ASS} =0.0V	10	11	–	Bits
LN		Linearity error	Vdd = 2.3 to 5.5V Ta=25℃	0	±4	±8	LSB
DNL		Differential nonlinear error	Vdd = 2.3 to 5.5V Ta=25℃	0	±0.5	±0.9	LSB
FSE		Full scale error	Vdd=V_{AREF}=5.0V, V_{ASS} =0.0V	±0	±4	±8	LSB
OE		Offset error	Vdd=V_{AREF}=5.0V, V_{ASS} =0.0V	±0	±2	±4	LSB
ZAI		Recommended impedance of analog voltage source	–	0	8	10	KΩ
TAD		ADC clock duration	Vdd=V_{AREF}=5.0V, V_{ASS} =0.0V	4	–	–	us
TCN		AD conversion time	Vdd=V_{AREF}=5.0V, V_{ASS} =0.0V	15	–	15	TAD
ADIV		ADC OP input voltage range	Vdd=V_{AREF}=5.0V, V_{ASS} =0.0V	0	–	V_{AREF}	V
ADOV		ADC OP output voltage swing	Vdd=V_{AREF}=5.0V, V_{ASS} =0.0V, RL=10KΩ	0	0.2	0.3	V
				4.7	4.8	5	
ADSR		ADC OP slew rate	Vdd=V_{AREF}=5.0V, V_{ASS} =0.0V	0.1	0.3	–	V/us
PSR		Power Supply Rejection	Vdd=5.0V±0.5V	±0	–	±2	LSB

Note: 1. These parameters are hypothetical (not tested) and are provided for design reference use only.
2. There is no current consumption when ADC is off other than minor leakage current.
3. AD conversion result will not decrease when an increase of input voltage and no missing code will result.
4. These parameters are subject to change without further notice.

8.2 Comparator (OP) Characteristic

Vdd = 5.0V, Vss=0V, Ta=25°C

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
SR	Slew rate	–	0.1	0.2		V/us
IVR	Input voltage range	Vdd =5.0V, V_{SS} =0.0V	0		5	V
OVS	Output voltage swing	Vd =5.0V, V_{SS} =0.0V, RL=10KΩ	0	0.2	0.3	V
			4.7	4.8	5	
Iop	Supply current of OP	–	250	350	500	μA
Ico	Supply current of Comparator	–	–	300	–	μA
PSRR	Power-supply Rejection Ration for OP	Vdd= 5.0V, V_{SS} =0.0V	50	60	70	dB
Vs	Operating range	–	2.5	–	5.5	V

Note: 1. These parameters are hypothetical (not tested) and are provided for design reference use only.
2. These parameters are subject to change without further notice.

8.3 Device Characteristics

The graphs below were derived based on a limited number of samples and they are provided for reference only. Hence, the device characteristic shown herein cannot be guaranteed as fully accurate. In these graphs, the data maybe out of the specified operating warranted range.

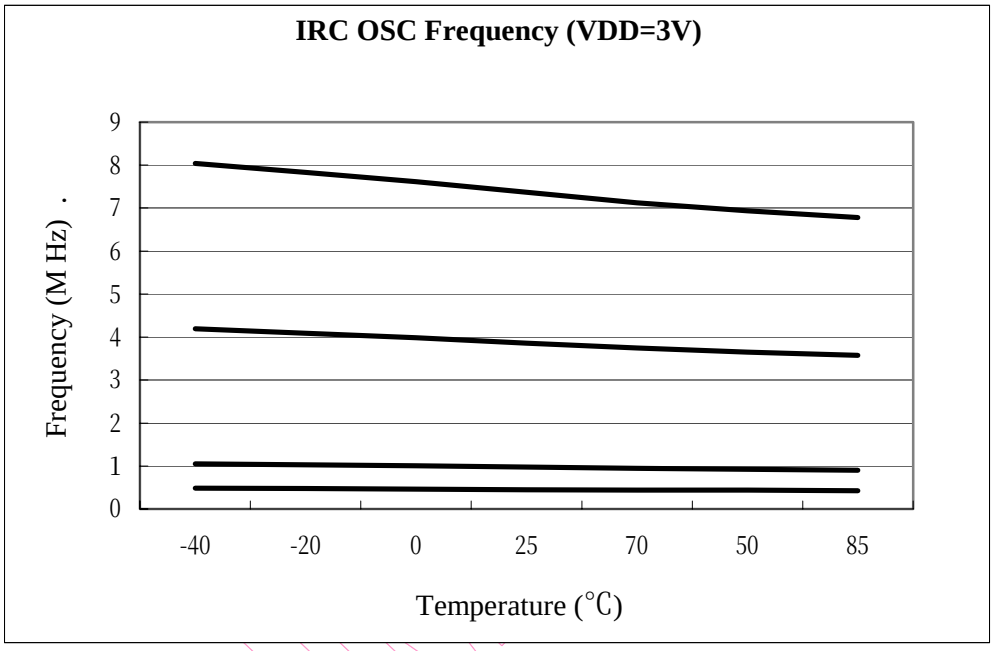


Fig. 8-1 Internal RC OSC Frequency vs. Temperature, VDD=3V

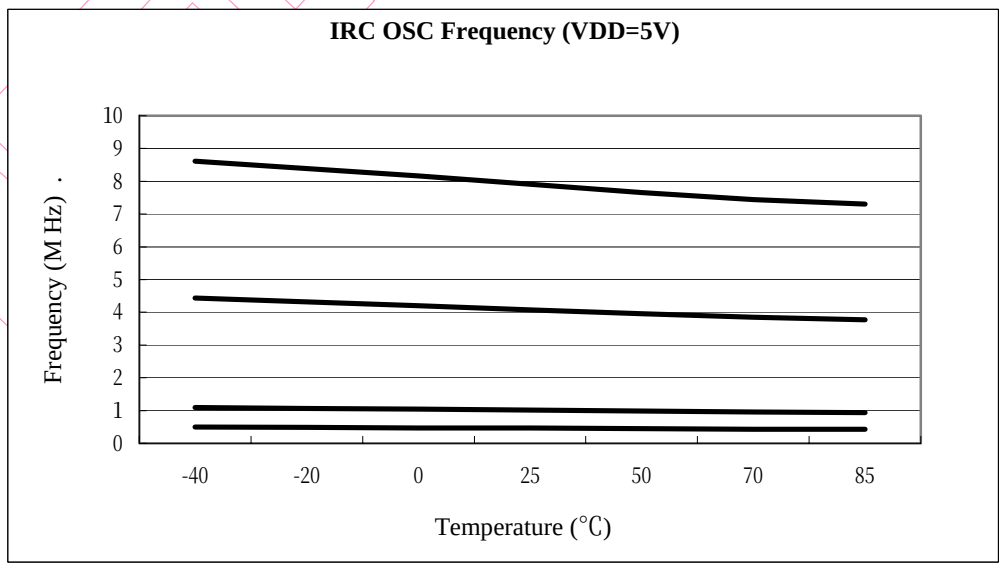


Fig. 8-2 Internal RC OSC Frequency vs. Temperature, VDD=5V

9 AC Electrical Characteristic

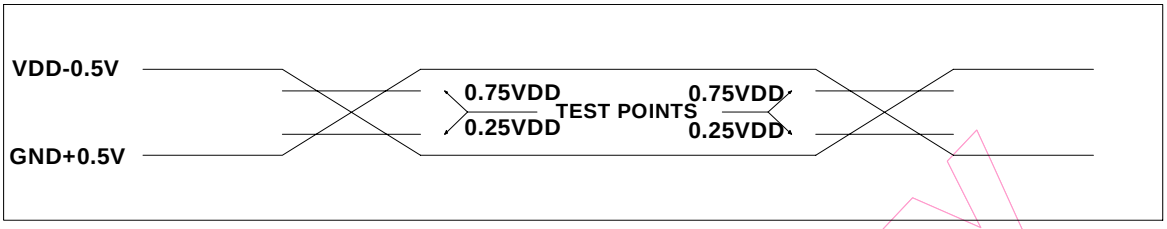
Ta=25 °C, VDD=5V±5%, VSS=0V

Symbol	Parameter	Conditions	Min	Type	Max	Unit
Dclk	Input CLK duty cycle	–	45	50	55	%
Tins	Instruction cycle time (CLKS="0")	Crystal type	100	–	DC	ns
		RC type	500	–	DC	ns
Ttcc	TCC input time period	–	(Tins+20) × N*	–	–	ns
Tdrh	Device reset hold time	Ta = 25°C	11.3	16.2	21.6	ms
Trst	/RESET pulse width	Ta = 25°C	2000			ns
Twdt	Watchdog timer duration	Ta = 25°C	11.3	16.2	21.6	ms
Tset	Input pin setup time	–	–	0		ns
Thold	Input pin hold time	–	15	20	25	ns
Tdelay	Output pin delay time	Cload=20pF	45	50	55	ns
Tdrc	ERC delay time	Ta = 25°C	1	3	5	ns

Note: * N = selected prescaler ratio

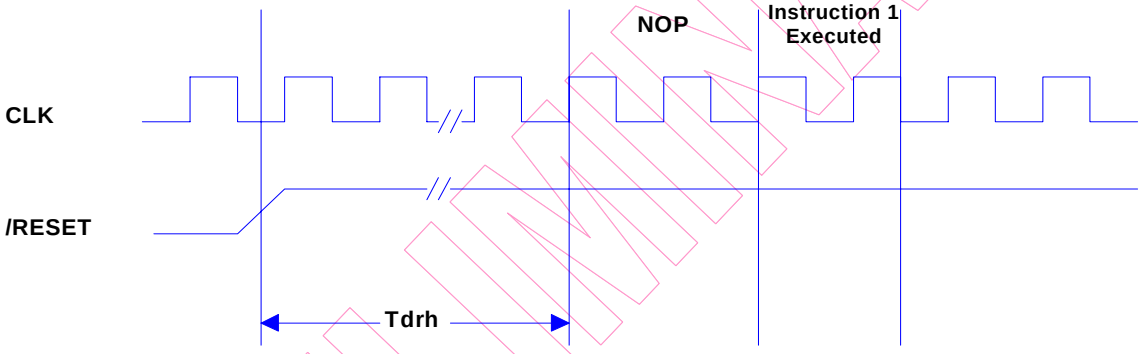
10 Timing Diagrams

AC Test Input/Output Waveform

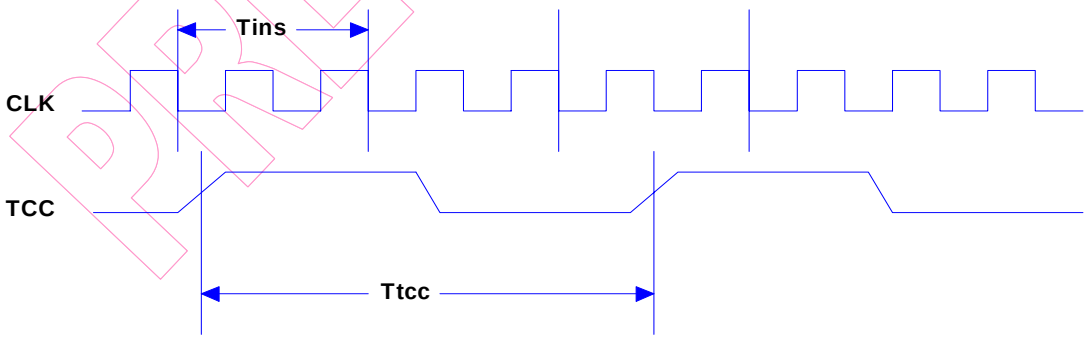


AC Testing : Input is driven at VDD-0.5V for logic "1",and GND+0.5V for logic "0".Timing measurements are made at 0.75VDD for logic "1",and 0.25VDD for logic "0".

RESET Timing (CLK="0")



TCC Input Timing (CLKS="0")



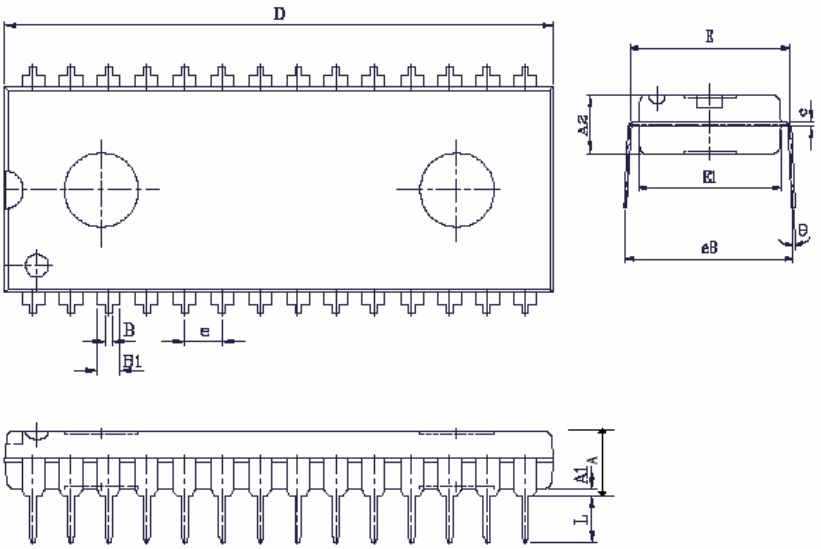
APPENDIX

A Package Type

OTP MCU	Package Type	Package size	Pin Count
EM78P350NP	DIP	600mil	28 pins
EM78P350NM	SOP	300mil	28 pins
EM78P350NK	SDIP	400mil	28 pins
EM78P350NAM	SDIP	300mil	28 pins
EM78P351NM	SOP	300mil	32 pins
EM78P351NK	Skinny DIP	400mil	32 pins
EM78P351NQ	LQFP	7*7m^2	32 pins
EM78P351NP	DIP	600mil	32 pins

B Packaging Configurations

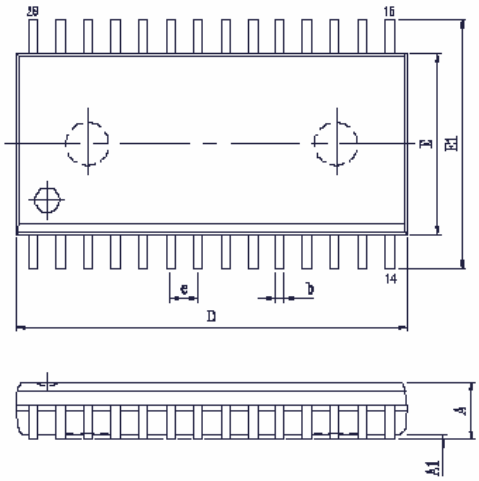
B.1 28-Lead Plastic Dual in line (PDIP) — 600 mil



Symbal	Min	Normal	Max
A			5.588
A1	0.381		
A2	3.683	3.937	4.191
c	0.254(TYP)		
D	36.830	37.084	37.338
E1	13.700	13.900	14.100
E	14.986	15.240	15.494
eB	15.412	16.256	17.100
B	0.356	0.457	0.559
B1	1.270	1.524	1.651
L	2.921	3.302	3.810
e	2.540(TYP)		
θ	0		15

TITLE: PDIP-28L 600MIL PACKAGE OUTLINE DIMENSION	
File : D28	Edtion: A
ELAN	Unit : mm
	Scale: Free
	Material:
	Sheet:1 of 1

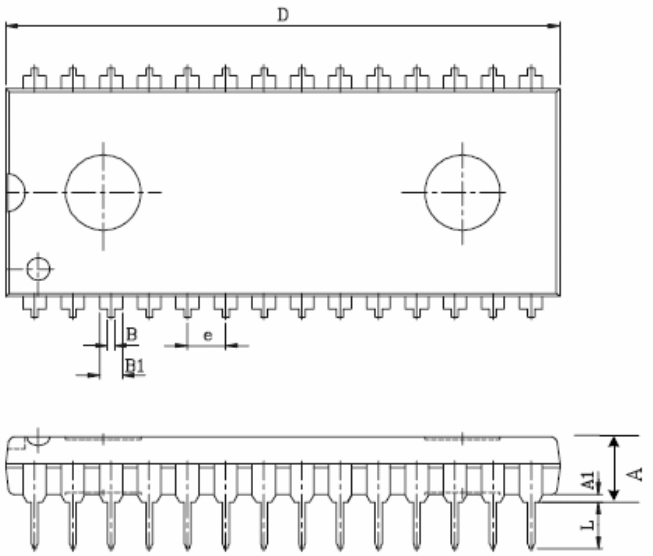
B.2 28-Lead Plastic Small Outline (SOP) — 300 mil



Symbal	Min	Normal	Max
A	2.370	2.500	2.630
A1	0.102		0.300
b	0.350	0.406	0.500
c		0.254(TYP)	
E	7.410	7.500	7.590
E1	10.000	10.325	10.650
D	17.700	17.900	18.100
L	0.678	0.881	1.084
L1	1.194	1.397	1.600
e		1.27(TYP)	
θ°	0		8

TITLE: SOP-28L(300MIL) PACKAGE OUTLINE DIMENSION	
File : SO28	Edtion: A
	Unit : mm
	Scale: Free
	Material:
	Sheet:1 of 1

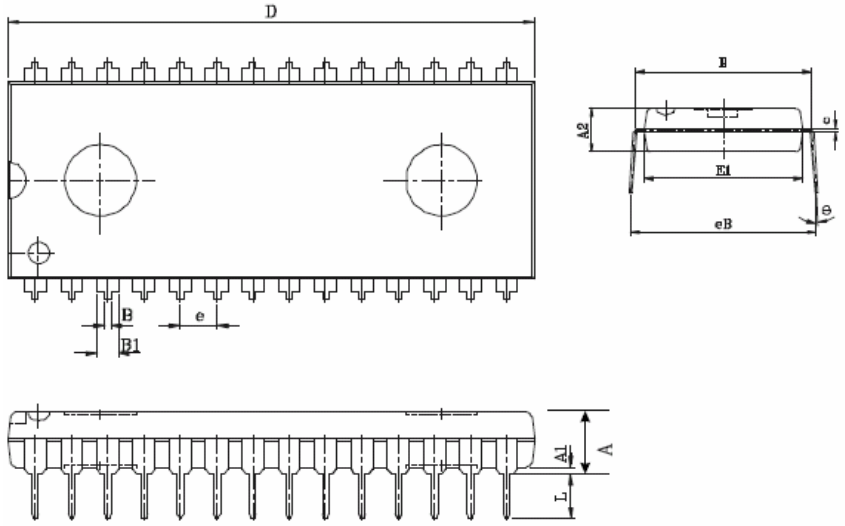
B.3 28-Lead Plastic Dual in line (PDIP) — 400 mil



Symbol	Min	Nomal	Max
A			4.360
A1	0.500		
B	0.380	0.460	0.540
B1	0.920	1.000	1.080
c	0.200	0.250	0.300
E		10.160	
E1	8.640	8.890	9.140
L	3.000		
e		1.778	
θ	0		10

TITLE: PDIP-28L SKINNY 40 0MIL PACKAGE OUTLINE DIME NSION	
File : K28A	Edtion: A
	Unit : mm
	Scale: Free
	Material:
	Sheet:1 of 1

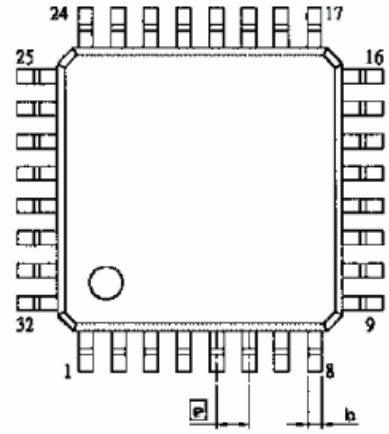
B.4 28-Lead Plastic Dual in line (PDIP) — 300 mil

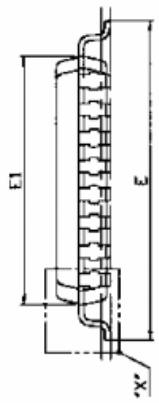


Symbal	Min	Normal	Max
A			5.334
A1	0.381		
A2	3.175	3.302	3.429
c	0.152	0.254	0.356
D	35.204	35.255	35.306
E1	7.213	7.315	7.417
E	7.620	7.874	8.128
eB	8.382	8.890	9.398
B	0.356	0.457	0.559
B1	1.422	1.524	1.626
L	3.251	3.302	3.353
e	2.540(TYP)		
θ	0		10

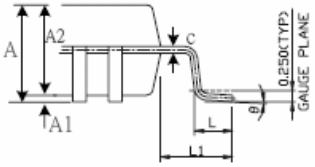
TITLE: PDIP-28L SKINNY 300MIL PACKAGE OUTLINE DIMENSION	
File : K28	Edition: A
	Unit : mm
	Scale: Free
	Material:
	Sheet:1 of 1

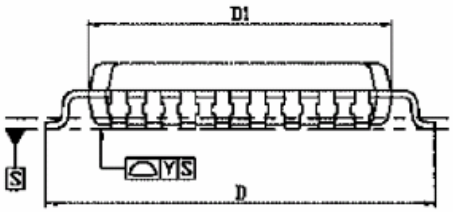
B.5 32-LQFP — 7x7m^2





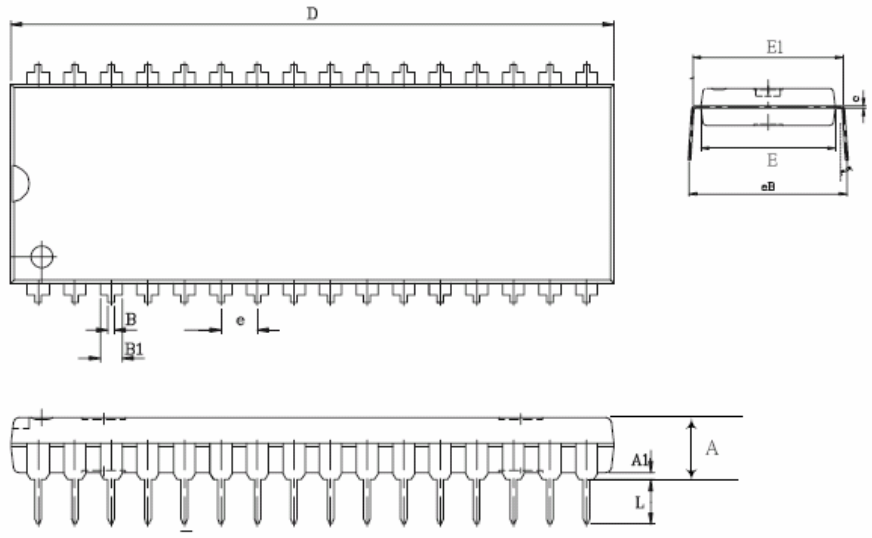
Symbal	Min	Normal	Max
A			1.60
A1	0.05		0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
c	0.09		0.20
D	9.00 BASIC		
D1	7.00 BASIC		
E	9.00 BASIC		
E1	7.00 BASIC		
L	0.45	0.60	0.75
L1	1.0(BASIC)		
e	0.8(BASIC)		
θ°	0	3.5	7





TITLE: LQFP-3 2 L(7*7 MM) FOOTPRINT 2.0mm PACKAGE OUTLINE DIMENSION	
File : LQFP32	Edtion: A
	Unit : mm
	Scale: Free
	Material:
	Sheet:1 of 1

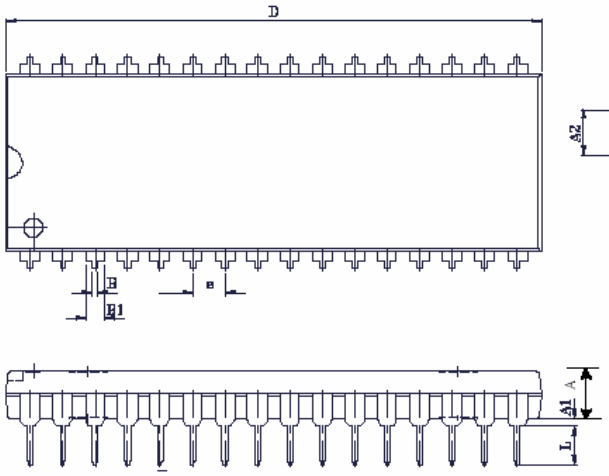
B.6 32-Lead Plastic Dual in line (PDIP) —400 mil



Symbal	Min	Normal	Max
A	4.50	4.70	4.90
A1	0.51		
c	0.20	0.25	0.30
D	28.20	28.30	28.40
E	8.79	8.89	8.99
E1		10.16	
eB	10.96	11.36	11.76
B	0.38	0.46	0.54
B1	0.50	1.00	1.50
L		3.00	
e		1.78	

TITLE: SD-32L(SKIN NY400 MIL) PACKAGE OUTLINE DI MENSION	
File : K32A	Edtion: A
	Unit : mm
	Scale: Free
	Material:
	Sheet:1 of 1

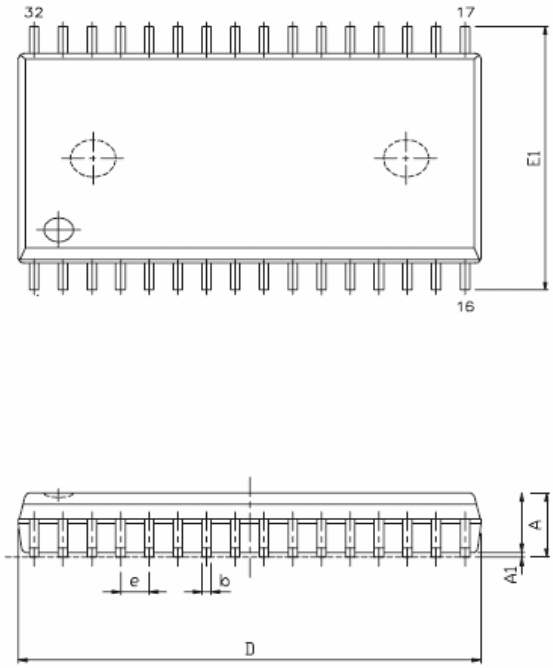
B.7 32-Lead Plastic Dual in line (PDIP) —600 mil



Symbal	Min	Normal	Max
A			5.588
A1	0.381		
A2	3.175	3.937	4.953
c		0.254(TYP)	
D	41.783	41.910	42.164
E1	13.700	13.900	14.100
E	14.986	15.240	15.494
eB	15.412	16.256	17.100
B	0.330	0.457	0.584
B1	1.143	1.270	1.397
L	2.921	3.302	3.810
e		2.540(TYP)	
θ	0		15

TITLE: PDIP-32L 600MIL PACKAGE OUTLINE DIMENSION	
File : D32	Edtion: A
	Unit : mm
	Scale: Free
	Material:
	Sheet:1 of 1

B.8 32-Lead Plastic Small Outline (SOP) — 300 mil



	EMC		
Symbol	Min	Normal	Max
A		2.54	
A1	0.1	0.15	0.2
b	0.3	0.4	0.5
c	0.2	0.25	0.3
E	7.4	7.5	7.6
E1	10.2	10.4	10.6
D	20.88	20.98	21.08
L	0.55	0.75	0.95
e		1.27	

TITLE: SOP-32L(300 MIL) PA CKAGE OUTLINE DIMENSI ON	
File : SO32 L	Edtion: A
	Unit : mm
	Scale: Free
	Material:
	Sheet:1 of 1

C Quality Assurance and Reliability

Test Category	Test Conditions	Remarks
Solderability	Solder temperature = 255 ± 5°C, for 5 seconds up to the stopper using a rosin-type flux	–
Pre-condition	Step 1: TCT, 65°C (15mins) ~ 150°C (15mins), 10 cycles	For SMD IC (such as SOP, QFP, SOJ, etc)
	Step 2: Bake at 125°C, TD (endurance) = 24 hrs	
	Step 3: Soak at 30°C / 60% , TD (endurance) = 192 hrs	
	Step 4: IR flow 3 cycles (Pkg thickness ≥ 2.5mm or Pkg volume ≥ 350 mm3 ----235 ± 5°C) (Pkg thickness ≤ 2.5 mm or Pkg volume ≤ 350 mm3 ----250 ± 5°C)	
Temperature cycle test	-65℃ (15mins)~150°C (15mins), 200 cycles	–
Pressure cooker test	TA =121°C, RH=100%, pressure=2 atm, TD (endurance)= 96 hrs	–
High temperature / High humidity test	TA=85°C , RH=85%, TD (endurance) = 168, 500 hrs	–
High-temperature storage life	TA=150°C, TD (endurance) = 500, 1000 hrs	–
High-temperature operating life	TA=125°C, VCC = Max. operating voltage, TD (endurance) = 168, 500, 1000 hrs	–
Latch-up	TA=25°C, VCC = Max. operating voltage, 600 ma / 40V	–
ESD (HBM)	TA=25°C, ≥ ｜± 4KV｜	IP_ND,OP_ND,IO_ND IP_NS,OP_NS,IO_NS IP_PD,OP_PD,IO_PD, IP_PS,OP_PS,IO_PS, VDD-VSS(+),VDD_VSS(-) mode
ESD (MM)	TA=25°C, ≥ ｜± 400V｜	

C.1 Address Trap Detect

An address trap detect is one of the MCU embedded fail-safe functions that detects MCU malfunction caused by noise or the like. Whenever the MCU attempts to fetch an instruction from a certain section of ROM, an internal recovery circuit is auto started. If a noise caused address error is detected, the MCU will repeat execution of the program until the noise is eliminated. The MCU will then continue to execute the next program.