MOSFET - P-Channel Logic Level PowerTrench®

-40 V, 13.5 mΩ, -50 A

FDD9510L-F085

ON Semiconductor®

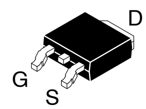
www.onsemi.com

Features

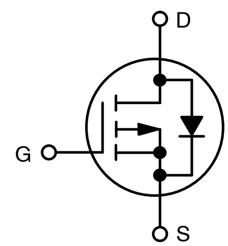
- Typ $R_{DS(on)}$ = 11 mΩ at V_{GS} = −10 V; I_D = −50 A
- Typ $Q_{g(tot)}$ = 28 nC at V_{GS} = −10 V; I_D = −50 A
- UIS Capability
- Qualified to AEC Q101
- These Devices are Pb−Free and are RoHS Compliant

Applications

- Automotive Engine Control
- Powertrain Management
- Solenoid and Motor Drivers
- Electrical Power Steering
- Integrated Starter/Alternator
- Distributed Power Architectures and VRM
- Primary Switch for 12 V Systems



DPAK
TO−252
CASE 369AS



ABSOLUTE MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain to Source Voltage	V_{DSS}	−40	V
Gate to Source Voltage	V_{GS}	±16	V
Drain Current − Continuous (V_{GS} = −10 V) (T_C = 25°C) (Note 1)	I_D	−50	A
Pulsed Drain Current (T_C = 25°C)	I_D	See Figure 4	A
Single Pulse Avalanche Energy (Note 2)	E_{AS}	35.3	mJ
Power Dissipation	P_D	75	W
Derate above 25°C	P_D	0.5	W/°C
Operating and Storage Temperature Range	T_J, T_{STG}	−55 to +175	°C
Thermal Resistance (Junction to Case)	$R_{\theta JC}$	2	°C/W
Maximum Thermal Resistance (Junction to Ambient) (Note 3)	$R_{\theta JA}$	52	°C/W

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Current is limited by wirebond configuration
2. Starting Tj = 25°C, L = 40 μH, I_{AS} = −42 A, V_{DD} = −40 V during inductor charging and V_{DD} = 0 V during time in avalanche
3. $R_{\theta JA}$ is the sum of the junction−to−case and case−to−ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design. The maximum rating presented here is based on mounting on a 1 in^2 pad of 2 oz copper.

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

PACKAGE MARKING AND ORDERING INFORMATION

Device	Device Marking	Package	Reel Size	Tape Width	Quantity
FDD9510L−F085	FDD9510L	D−PAK (TO−252)	13″	16 mm	2500 Units

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
BV_{DSS}	Drain to Source Breakdown Voltage	V_{GS} = 0 V, I_D = −250 μA		−40	–	–	V
I_{DSS}	Drain to Source Leakage Current	V_{DS} = −40 V, V_{GS} = 0 V	T_J = 25°C	–	–	−1	μA
			T_J = 175°C (Note 4)	–	–	−1	mA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±16 V		–	–	±100	nA
ON CHARACTERISTICS							
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA		−1	−1.9	−3	V
$R_{DS(on)}$	Drain to Source On−Resistance	V_{GS} = −4.5 V, I_D = −50 A, T_J = 25°C		–	16	22	mΩ
		V_{GS} = −10 V, I_D = −50 A	T_J = 25°C	–	11	13.5	mΩ
			T_J = 175°C (Note 4)	–	18	22.7	mΩ
DYNAMIC CHARACTERISTICS							
C_{iss}	Input Capacitance	V_{DS} = −20 V, V_{GS} = 0 V, f = 1 MHz		–	2020	–	pF
C_{oss}	Output Capacitance			–	785	–	pF
C_{rss}	Reverse Transfer Capacitance			–	36	–	pF
R_g	Gate Resistance	V_{GS} = −0.5 V, f = 1 MHz		–	23	–	Ω
$Q_{g(tot)}$	Total Gate Charge	V_{DD} = −20 V, I_D = −50 A	V_{GS} = 0 V to −10 V	–	28	37	nC
$Q_{g(-4.5)}$	Total Gate Charge		V_{GS} = 0 V to −4.5 V	–	13	–	nC
$Q_{g(th)}$	Threshold Gate Charge		V_{GS} = 0 V to −1 V	–	2	–	nC
Q_{gs}	Gate to Source Gate Charge	V_{DD} = −20 V, I_D = −50 A		–	7	–	nC
Q_{gd}	Gate to Drain “Miller” Charge			–	4	–	nC
SWITCHING CHARACTERISTICS							
t_{on}	Turn-On Time	V_{DD} = −20 V, I_D = −50 A, V_{GS} = −10 V, R_{GEN} = 6 Ω		–	–	44	ns
$t_{d(on)}$	Turn-On Delay Time			–	8	–	ns
t_r	Turn-On Rise Time			–	21	–	ns
$t_{d(off)}$	Turn-Off Delay Time			–	113	–	ns
t_f	Turn-Off Fall Time			–	35	–	ns
t_{off}	Turn-Off Time			–	–	220	ns
DRAIN−SOURCE DIODE CHARACTERISTICS							
V_{SD}	Source to Drain Diode Voltage	V_{GS} = 0 V, I_{SD} = −50 A		–	−0.97	−1.25	V
		V_{GS} = 0 V, I_{SD} = −25 A		–	−0.9	−1.2	V
T_{rr}	Reverse Recovery Time	I_F = −50 A, dI_{SD}/dt = 100 A/μs		–	42	63	ns
Q_{rr}	Reverse Recovery Charge			–	31	56	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. The maximum value is specified by design at T_J = 175°C. Product is not tested to this condition in production

TYPICAL CHARACTERISTICS

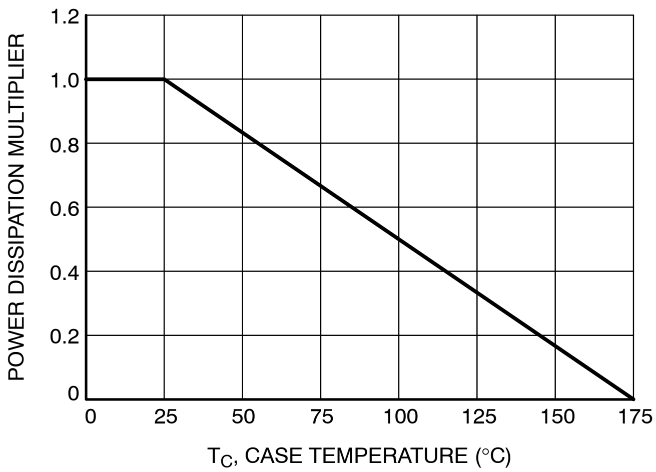


Figure 1. Normalized Power Dissipation vs. Case Temperature

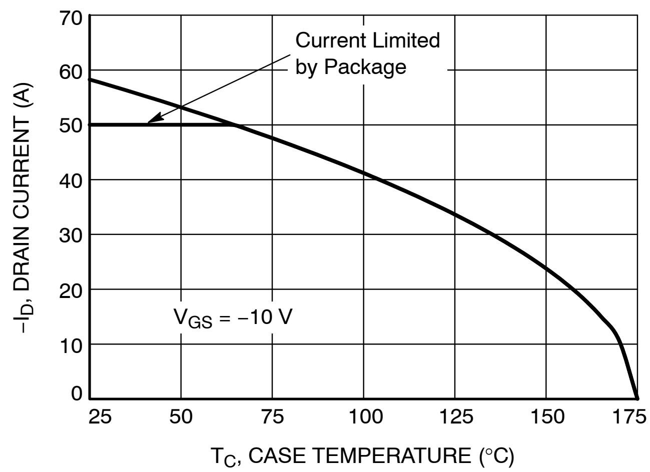


Figure 2. Maximum Continuous Drain Current vs. Case Temperature

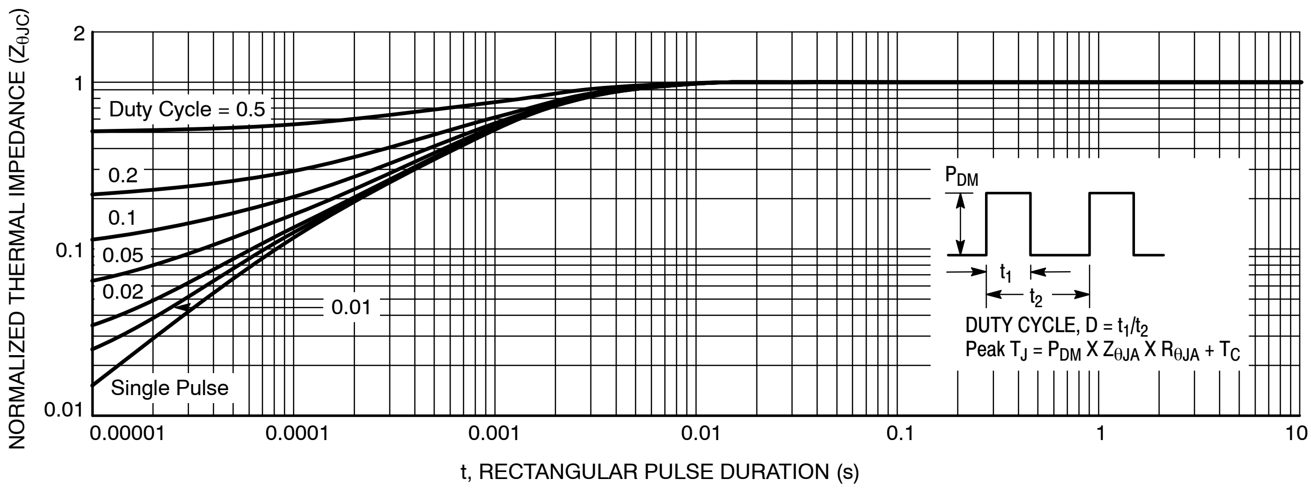


Figure 3. Normalized Maximum Transient Thermal Impedance

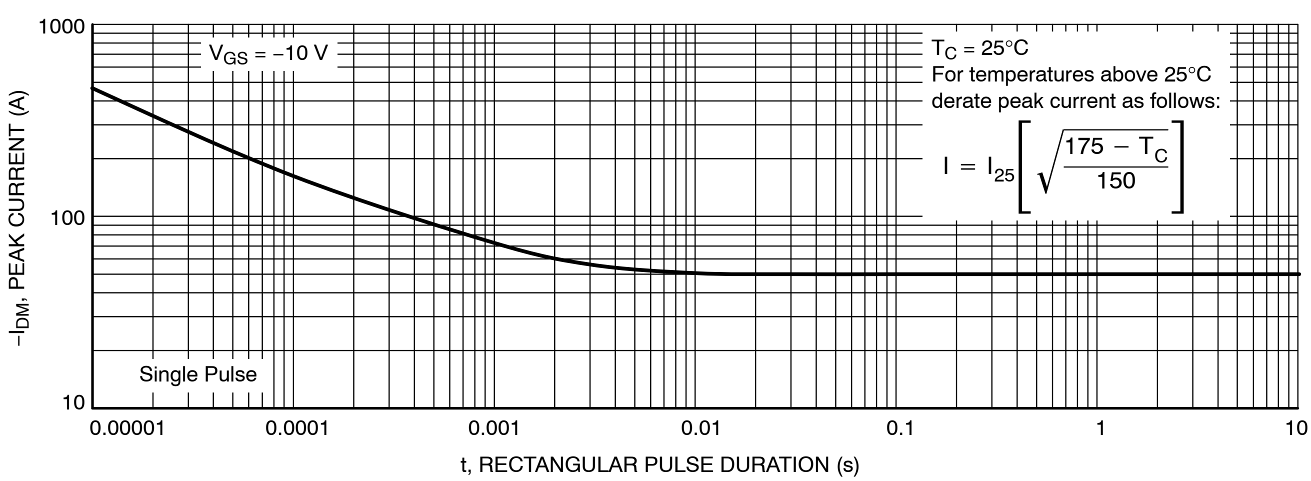


Figure 4. Peak Current Capability

TYPICAL CHARACTERISTICS

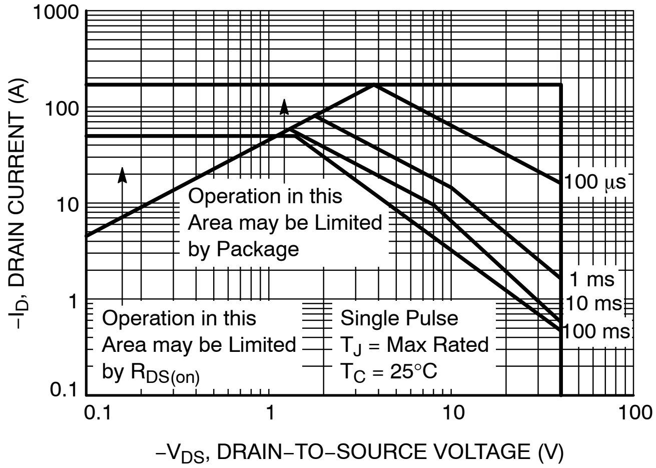


Figure 5. Forward Bias Safe Operating Area

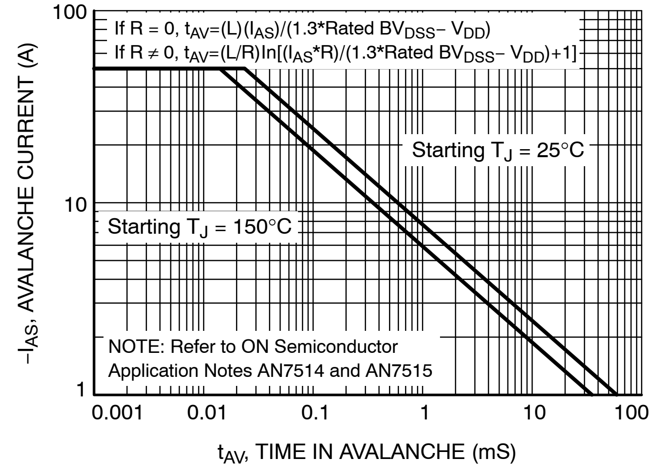


Figure 6. Unclamped Inductive Switching Capability

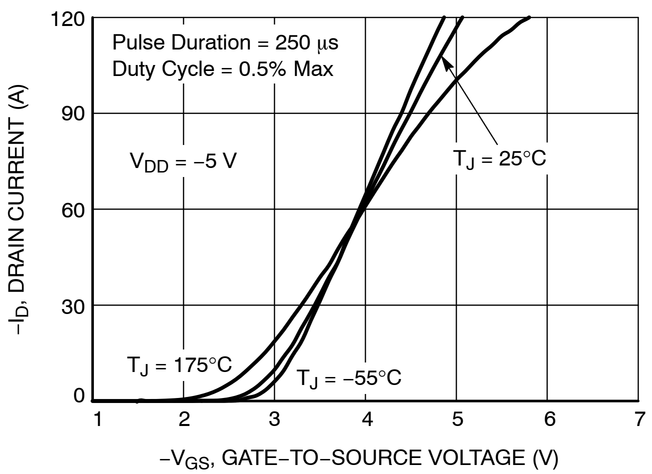


Figure 7. Transfer Characteristics

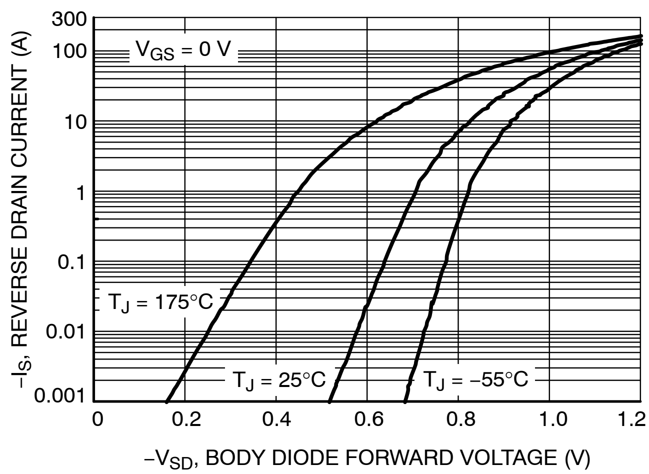


Figure 8. Forward Diode Characteristics

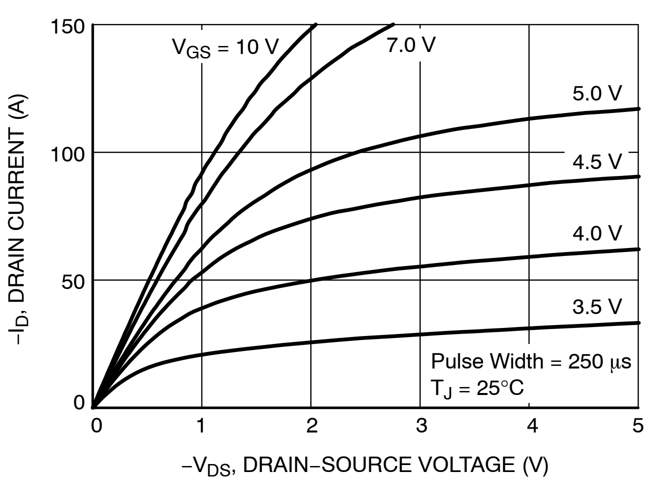


Figure 9. Saturation Characteristics

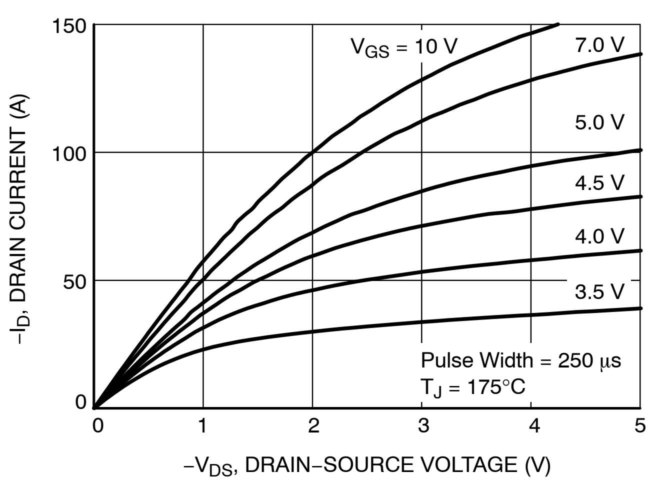


Figure 10. Saturation Characteristics

TYPICAL CHARACTERISTICS

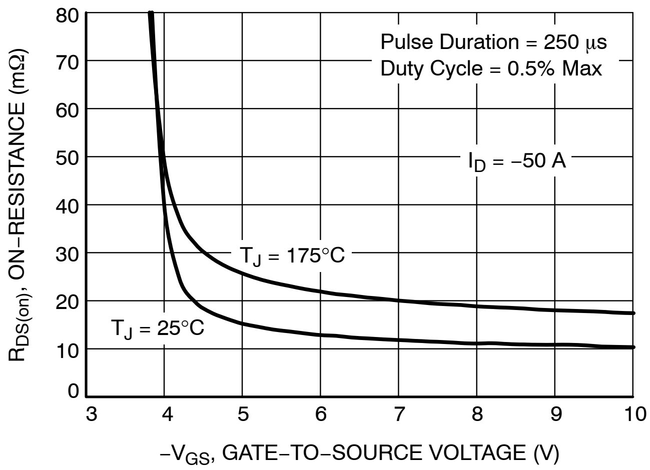


Figure 11. $R_{DS(on)}$ vs. Gate Voltage

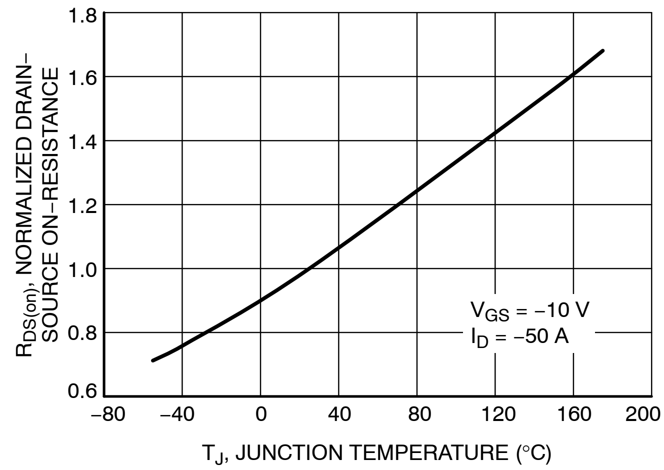


Figure 12. Normalized $R_{DS(on)}$ vs. Junction Temperature

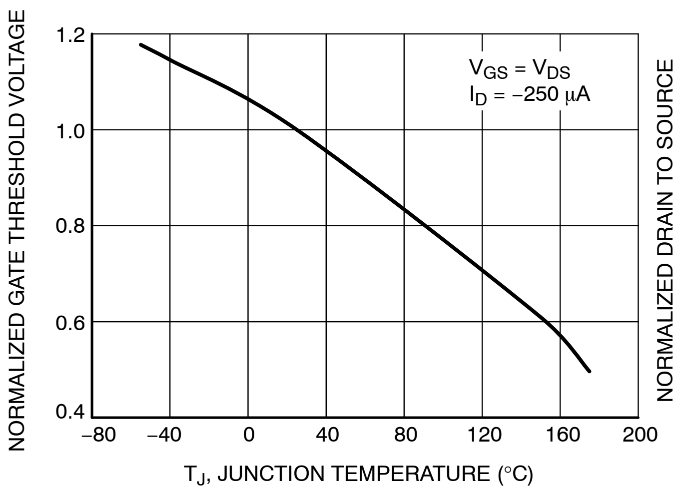


Figure 13. Normalized Gate Threshold Voltage vs. Temperature

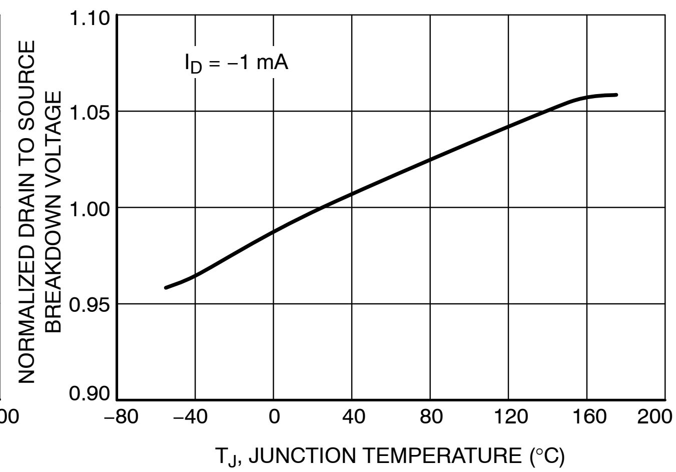


Figure 14. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

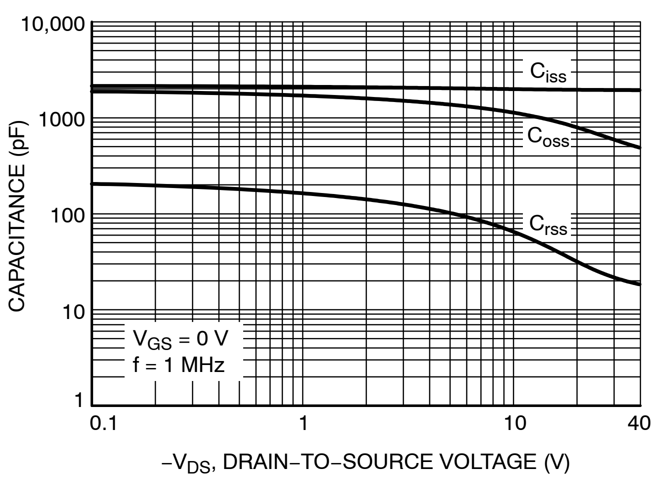


Figure 15. Capacitance vs. Drain to Source Voltage

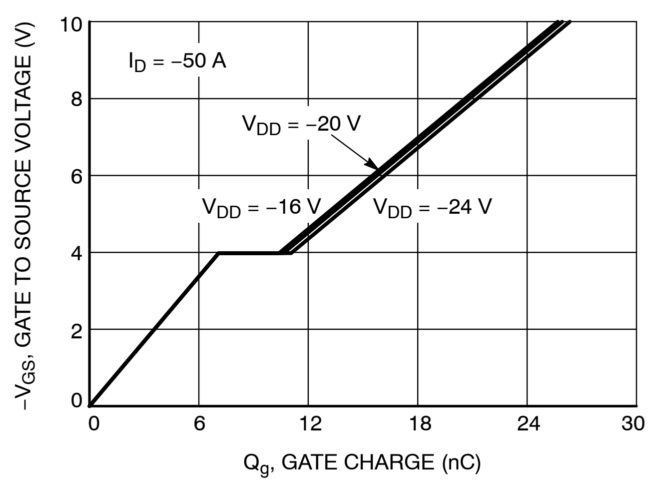


Figure 16. Gate Charge vs. Gate to Source Voltage

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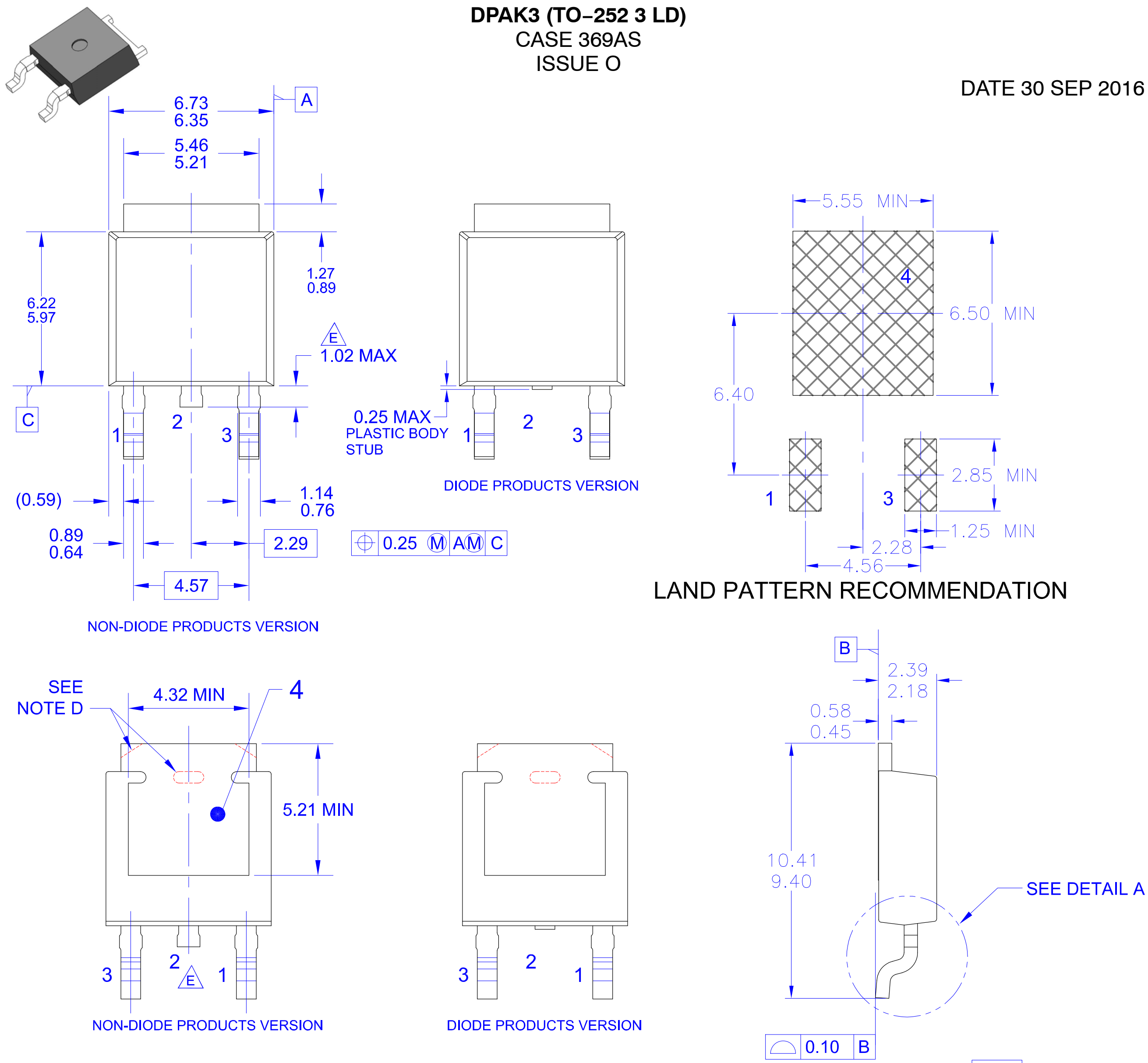
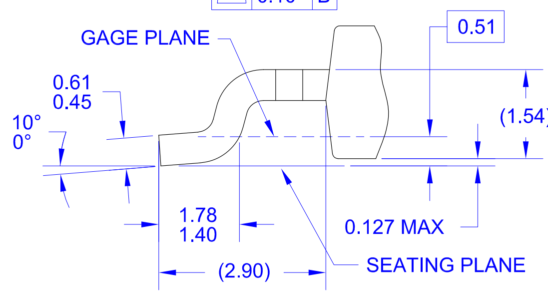


NOTES: UNLESS OTHERWISE SPECIFIED
- A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
- D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION.
- E) TRIMMED CENTER LEAD IS PRESENT ONLY FOR DIODE PRODUCTS
- F) DIMENSIONS ARE EXCLUSSIVE OF BURSS, MOLD FLASH AND TIE BAR EXTRUSIONS.
- G) LAND PATTERN RECOMENDATION IS BASED ON IPC7351A STD TO228P991X239-3N.



DETAIL A
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DESCRIPTION:	**DPAK3 (TO−252 3 LD)**	**PAGE 1 OF 1**

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