**FAIRCHILD**

SEMICONDUCTOR ™

# FDS6614A

## N-Channel Logic Level PowerTrench™ MOSFET

### General Description

This N-Channel Logic Level MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize on-state resistance and yet maintain superior switching performance.

These devices are well suited for low voltage and battery powered applications where low in-line power loss and fast switching are required.

### Applications

- DC/DC converter
- Load switch
- Motor drives

### Features

- 9.3 A, 30 V. $R_{DS(ON)} = 0.018 \ \Omega$ @ $V_{GS} = 10$ V
  $R_{DS(ON)} = 0.025 \ \Omega$ @ $V_{GS} = 4.5$ V

- Low gate charge (12nC typical).

- Fast switching speed.

- High performance trench technology for extremely low $R_{DS(ON)}$.

- High power and current handling capability.



SO-8
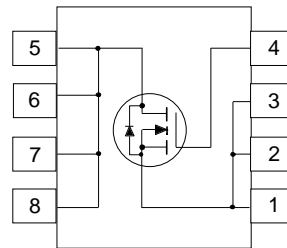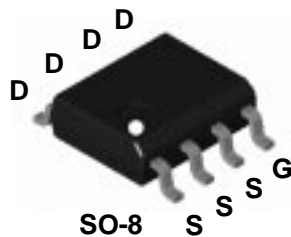


## Absolute Maximum Ratings $T_A = 25°C$ unless otherwise noted

| Symbol | Parameter | | Ratings | Units |
|--------|-----------|--|---------|-------|
| $V_{DSS}$ | Drain-Source Voltage | | 30 | V |
| $V_{GSS}$ | Gate-Source Voltage | | $\pm20$ | V |
| $I_D$ | Drain Current  - Continuous | (Note 1a) | 9.3 | A |
| | - Pulsed | | 40 | |
| $P_D$ | Power Dissipation for Single Operation | (Note 1a) | 2.5 | W |
| | | (Note 1b) | 1.2 | |
| | | (Note 1c) | 1 | |
| $T_J$, $T_{stg}$ | Operating and Storage Junction Temperature Range | | -55 to +150 | °C |

## Thermal Characteristics

| | | | | |
|--------|-----------|--|---------|-------|
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient | (Note 1a) | 50 | °C/W |
| $R_{\theta JC}$ | Thermal Resistance, Junction-to-Case | (Note 1) | 25 | °C/W |

## Package Outlines and Ordering Information

| Device Marking | Device | Reel Size | Tape Width | Quantity |
|----------------|--------|-----------|------------|----------|
| FDS6614A | FDS6614A | 13" | 12mm | 2500 units |

FDS6614A Rev. B

## Electrical Characteristics    $T_A$ = 25°C unless otherwise noted

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|--------|-----------|-----------------|-----|-----|-----|-------|
| **Off Characteristics** | | | | | | |
| $BV_{DSS}$ | Drain-Source Breakdown Voltage | $V_{GS}$ = 0 V, $I_D$ = 250 μA | 30 | | | V |
| $\frac{\Delta BV_{DSS}}{\Delta T_J}$ | Breakdown Voltage Temperature Coefficient | $I_D$ = 250 μA, Referenced to 25°C | | 24 | | mV/°C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = 24 V, $V_{GS}$ = 0 V | | | 1 | μA |
| $I_{GSSF}$ | Gate-Body Leakage Current, Forward | $V_{GS}$ = 20 V, $V_{DS}$ = 0 V | | | 100 | nA |
| $I_{GSSR}$ | Gate-Body Leakage Current, Reverse | $V_{GS}$ = -20 V, $V_{DS}$ = 0 V | | | -100 | nA |
| **On Characteristics**   (Note 2) | | | | | | |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 μA | 1 | 1.6 | 3 | V |
| $\frac{\Delta V_{GS(th)}}{\Delta T_J}$ | Gate Threshold Voltage Temperature Coefficient | $I_D$ = 250 μA, Referenced to 25°C | | -4 | | mV/°C |
| $R_{DS(on)}$ | Static Drain-Source On-Resistance | $V_{GS}$ = 10 V, $I_D$ = 9.3 A<br>$V_{GS}$ = 10 V, $I_D$ = 9.3 A, $T_J$ = 125°C<br>$V_{GS}$ = 4.5 V, $I_D$ = 8 A | | 0.015<br>0.022<br>0.019 | 0.018<br>0.030<br>0.025 | Ω |
| $I_{D(on)}$ | On-State Drain Current | $V_{GS}$ = 10 V, $V_{DS}$ = 5 V | 20 | | | A |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$ = 5 V, $I_D$ = 9.3 A | | 26 | | S |
| **Dynamic Characteristics** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = 15 V, $V_{GS}$ = 0 V, f = 1.0 MHz | | 1160 | | pF |
| $C_{oss}$ | Output Capacitance | | | 250 | | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | | 100 | | pF |
| **Switching Characteristics**   (Note 2) | | | | | | |
| $t_{d(on)}$ | Turn-On Delay Time | $V_{DD}$ = 15 V, $I_D$ = 1 A, $V_{GS}$ = 10 V, $R_{GEN}$ = 6 Ω | | 9 | 17 | ns |
| $t_r$ | Turn-On Rise Time | | | 11 | 20 | ns |
| $t_{d(off)}$ | Turn-Off Delay Time | | | 23 | 37 | ns |
| $t_f$ | Turn-Off Fall Time | | | 8 | 16 | ns |
| $Q_g$ | Total Gate Charge | $V_{DS}$ = 15 V, $I_D$ = 9.3 A, $V_{GS}$ = 5 V, | | 12 | 17 | nC |
| $Q_{gs}$ | Gate-Source Charge | | | 3.2 | | nC |
| $Q_{gd}$ | Gate-Drain Charge | | | 3.7 | | nC |
| **Drain-Source Diode Characteristics and Maximum Ratings** | | | | | | |
| $I_S$ | Maximum Continuous Drain-Source Diode Forward Current | | | | 2.1 | A |
| $V_{SD}$ | Drain-Source Diode Forward Voltage | $V_{GS}$ = 0 V, $I_S$ = 2.1 A   (Note 2) | | 0.75 | 1.2 | V |

**Notes:**

**1:** $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.
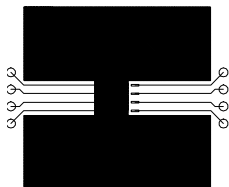
a) 50° C/W when mounted on a 1 in² pad of 2 oz. copper.
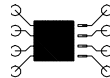
b) 105° C/W when mounted on a 0.04 in² pad of 2 oz. copper.
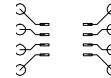
c) 125° C/W when mounted on a mimimum pad.

Scale  1 : 1  on letter size paper

**2:** Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%
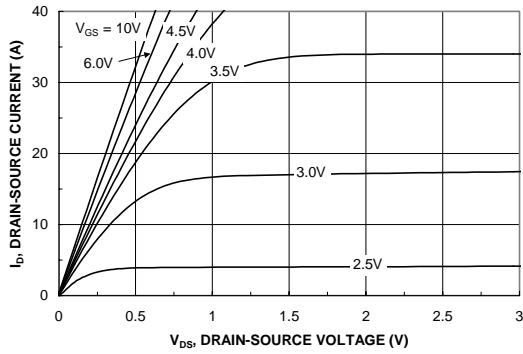
## Typical Characteristics



**Figure 1. On-Region Characteristics.**
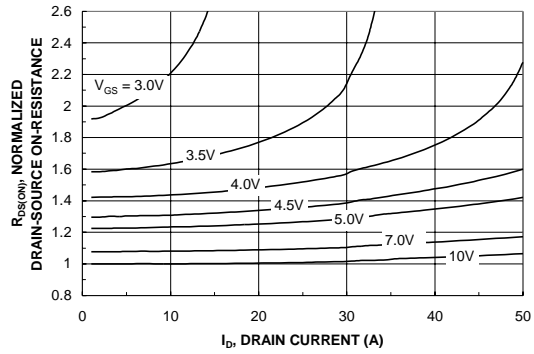


**Figure 2. On-Resistance Variation
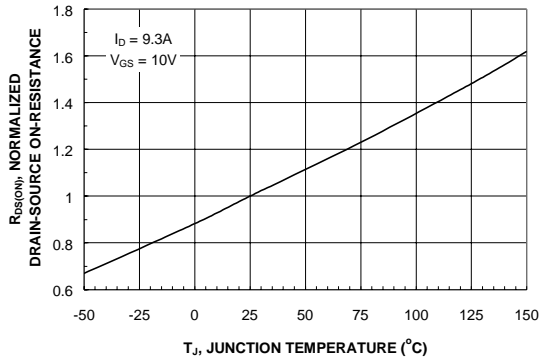with Drain Current and Gate Voltage.**



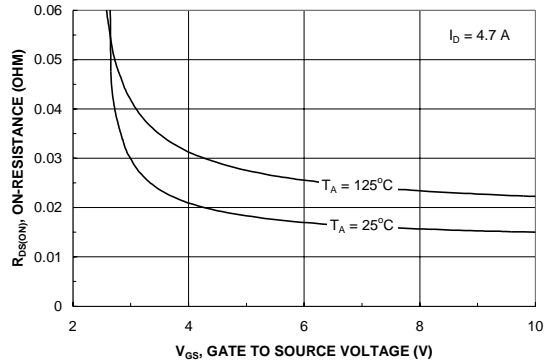**Figure 3. On-Resistance Variation
with Temperature.**



**Figure 4. On-Resistance Variation
with Gate-to-Source Voltage.**
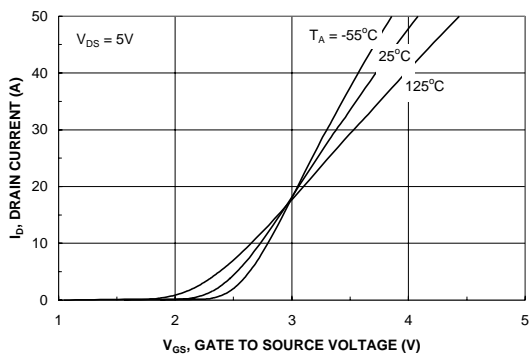


**Figure 5. Transfer Characteristics.**
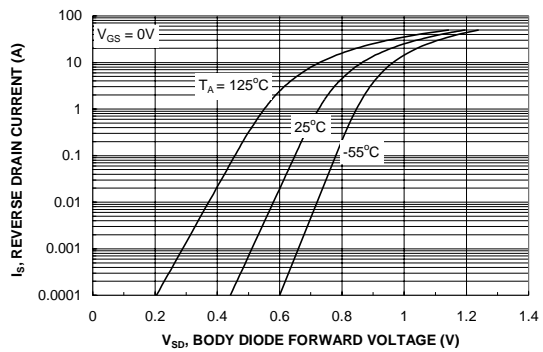


**Figure 6. Body Diode Forward Voltage Variation
with Source Current
and Temperature.**

# Typical Characteristics (continued)
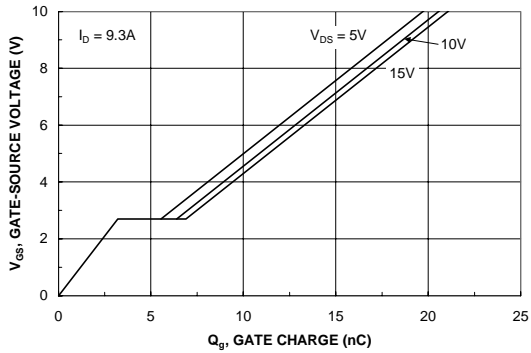


Figure 7. Gate-Charge Characteristics.
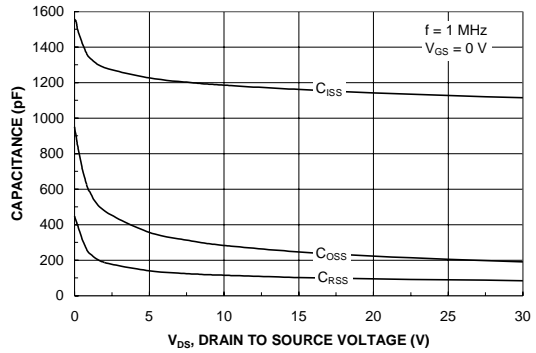


Figure 8. Capacitance Characteristics.
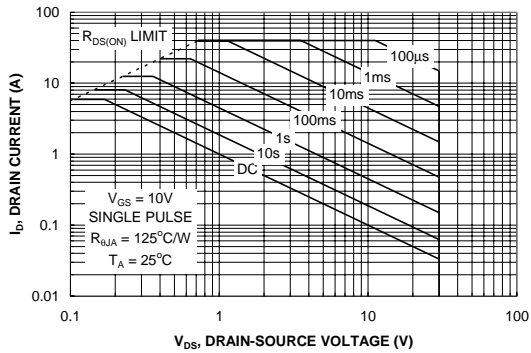


Figure 9. Maximum Safe Operating Area.



Figure 10. Single Pulse Maximum Power Dissipation.



Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c.
Transient thermal response will change depending on the circuit board design.

# SO-8 Tape and Reel Data and Package Dimensions

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## SOIC(8lds) Packaging
## Configuration: Figure 1.0

ESD Label

Antistatic Cover Tape

Static Dissipative
Embossed Carrier Tape

F63TNR
Label

Customized
Label

**Packaging Description:**

SOIC-8 parts are shipped in tape. The carrier tape is made from a dissipative (carbon filled) polycarbonate resin. The cover tape is a multilayer film (Heat Ac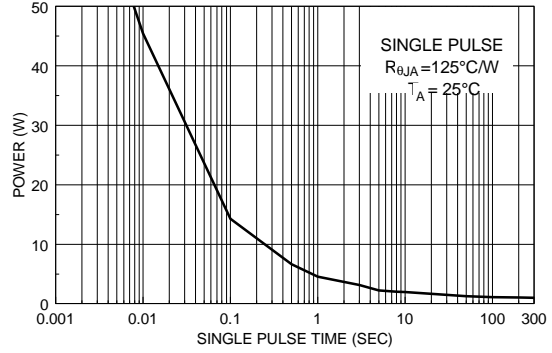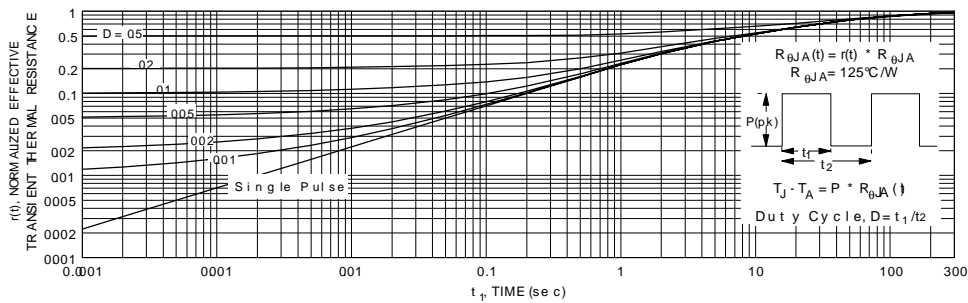tivated Adhesive in nature) primarily composed of polyester film, adhesive layer, sealant, and anti-static sprayed agent. These reeled parts in standard option are shipped with 2,500 units per 13" or 330cm diameter reel. The reels are dark blue in color and is made of polystyrene plastic (anti-static coated). Other option comes in 500 units per 7" or 177cm diameter reel. This and some other options are further described in the Packaging Information table.

These full reels are individually barcode labeled and placed inside a standard intermediate box (illustrated in figure 1.0) made of recyclable corrugated brown paper. One box contains two reels maximum. And these boxes are placed inside a barcode labeled shipping box which comes in different sizes depending on the number of parts shipped.
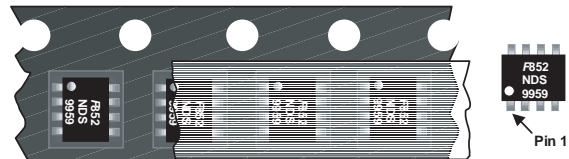
**SOIC-8 Unit Orientation**

Pin 1

### SOIC (8lds) Packaging Information

| Packaging Option | Standard (no flow code) | L86Z | F011 | D84Z |
|---|---|---|---|---|
| Packaging type | TNR | Rail/Tube | TNR | TNR |
| Qty per Reel/Tube/Bag | 2,500 | 95 | 4,000 | 500 |
| Reel Size | 13" Dia | - | 13" Dia | 7" Dia |
| Box Dimension (mm) | 343x64x343 | 530x130x83 | 343x64x343 | 184x187x47 |
| Max qty per Box | 5,000 | 30,000 | 8,000 | 1,000 |
| Weight per unit (gm) | 0.0774 | 0.0774 | 0.0774 | 0.0774 |
| Weight per Reel (kg) | 0.6060 | - | 0.9696 | 0.1182 |
| Note/Comments | | | | |

343mm x 342mm x 64mm
Standard Intermediate box

ESD Label

F63TN label

F63TN Label

ESD Label

F63TNR Label sample

LOT: CBVK741B019          QTY: 2500

FSID:  FDS9953A          SPEC:

D/C1: D9842     QTY1:     SPEC REV:
D/C2:           QTY2:     CPN:
                         N/F: F      (F63TNR)3

## SOIC(8lds) Tape Leader and Trailer
## Configuration: Figure 2.0

Carrier Tape

Cover Tape

Trailer Tape
640mm minimum or
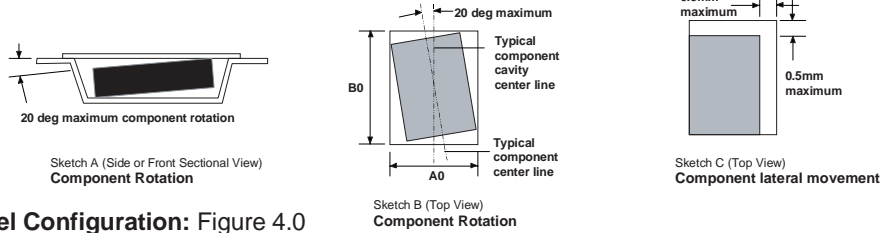80 empty pockets

Components

Leader Tape
1680mm minimum or
210 empty pockets

# SO-8 Tape and Reel Data and Package Dimensions, continued

## SOIC(8lds) Embossed Carrier Tape
**Configuration:** Figure 3.0

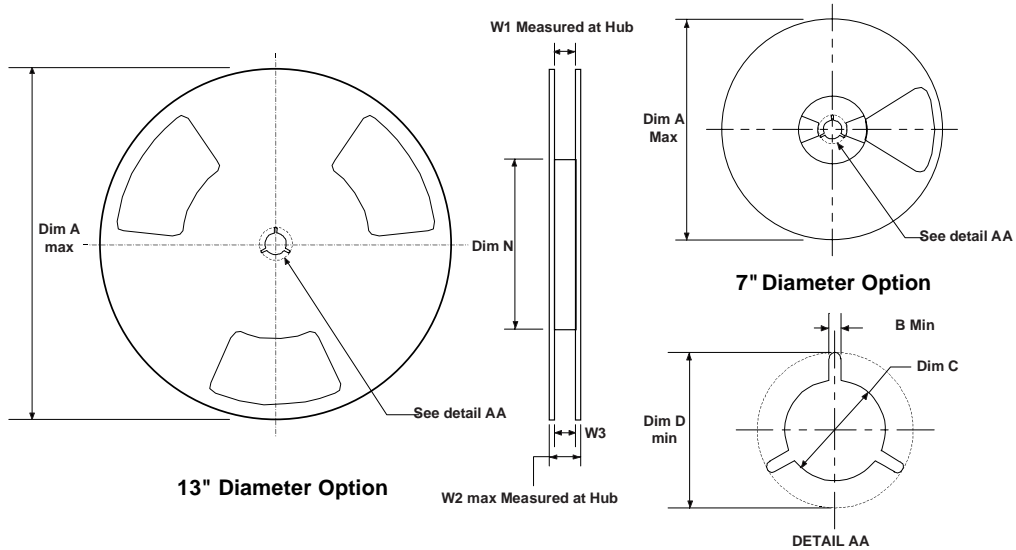T · P0 · D0 · E1 · F · E2 · W · K0 · Wc · B0 · Tc · A0 · P1 · D1

**User Direction of Feed**

| Dimensions are in millimeter | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Pkg type | A0 | B0 | W | D0 | D1 | E1 | E2 | F | P1 | P0 | K0 | T | Wc | Tc |
| SOIC(8lds) (12mm) | 6.50 +/-0.10 | 5.30 +/-0.10 | 12.0 +/-0.3 | 1.55 +/-0.05 | 1.60 +/-0.10 | 1.75 +/-0.10 | 10.25 min | 5.50 +/-0.05 | 8.0 +/-0.1 | 4.0 +/-0.1 | 2.1 +/-0.10 | 0.450 +/- 0.150 | 9.2 +/-0.3 | 0.06 +/-0.02 |

Notes: A0, B0, and K0 dimensions are determined with respect to the EIA/Jedec RS-481
rotational and lateral movement requirements (see sketches A, B, and C).

20 deg maximum component rotation

Sketch A (Side or Front Sectional View)
**Component Rotation**

20 deg maximum
Typical component cavity center line
B0
A0
Typical component center line

Sketch B (Top View)
**Component Rotation**

0.5mm maximum
0.5mm maximum

Sketch C (Top View)
**Component lateral movement**

## SOIC(8lds) Reel Configuration: Figure 4.0

W1 Measured at Hub

Dim A max
Dim N
See detail AA
**13" Diameter Option**
W3
W2 max Measured at Hub

Dim A Max
See detail AA
**7" Diameter Option**

B Min
Dim C
Dim D min
**DETAIL AA**

| Dimensions are in inches and millimeters | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Tape Size | Reel Option | Dim A | Dim B | Dim C | Dim D | Dim N | Dim W1 | Dim W2 | Dim W3 (LSL-USL) |
| 12mm | 7" Dia | 7.00 177.8 | 0.059 1.5 | 512 +0.020/-0.008 13 +0.5/-0.2 | 0.795 20.2 | 2.165 55 | 0.488 +0.078/-0.000 12.4 +2/0 | 0.724 18.4 | 0.469 – 0.606 11.9 – 15.4 |
| 12mm | 13" Dia | 13.00 330 | 0.059 1.5 | 512 +0.020/-0.008 13 +0.5/-0.2 | 0.795 20.2 | 7.00 178 | 0.488 +0.078/-0.000 12.4 +2/0 | 0.724 18.4 | 0.469 – 0.606 11.9 – 15.4 |

# SOIC-8 (FS PKG Code S1)

Scale 1:1 on letter size paper

Dimensions shown below are in:
inches [millimeters]

Part Weight per unit (gram): 0.0774



−B−  ⟨2⟩   0.1968 ⎡5.00⎤
               0.1890 ⎣4.80⎦

LEAD NO. 1
IDENTIFICATION

−C−  0.1574 ⎡4.00⎤
       0.1497 ⎣3.80⎦

8 7 6 5

0.2440 ⎡6.20⎤
0.2284 ⎣5.80⎦     −C− ⟨2⟩

1 2 3 4

0.0500 [1.27]     0.0200 ⎡0.51⎤
                     0.0138 ⎣0.35⎦ TYP.

⟨3⟩ ⊕ 0.010[0.25]Ⓜ [0.25] A CⓈ B

0.0200 [0.51]

0.2260 [5.74]

0.0390 [0.99]

0.0500 [1.27]

LAND PATTERN RECOMMENDATION

0.0688 ⎡1.75⎤
0.0532 ⎣1.35⎦

0.0098 ⎡0.25⎤
0.0040 ⎣0.10⎦

45° 0.0196 ⎡0.50⎤
        0.0099 ⎣0.25⎦

0.0098 ⎡0.25⎤
0.0075 ⎣0.19⎦

SEATING PLANE     −A−

GAGE PLANE

⟨3⟩ 0.0140 [0.36]

⌓ 0.004[0.10]
ALL LEAD TIPS

8°MAX. TYP.ALL LEADS

0.0500 ⎡1.27⎤
0.0160 ⎣0.41⎦ TYP. ALL LEADS

NOTES : UNLESS OTHERWISE SPECIFIED

1. STANDARD LEAD FINISH:
   200 MICROINCHES / 5.08 MICRONS MINIMUM
   LEAD / TIN (SOLDER) ON COPPER.

SO 0.150 WIDE 8 LEADS

⟨2⟩ THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH

⟨3⟩ MAXIMUM LEAD 0.024 [0.609]

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| CoolFET™ | MICROWIRE™ | TinyLogic™ |
| CROSSVOLT™ | POP™ | UHC™ |
| E²CMOS™ | PowerTrench® | VCX™ |
| FACT™ | QFET™ | |
| FACT Quiet Series™ | QS™ | |
| FAST® | Quiet Series™ | |
| FASTr™ | SuperSOT™-3 | |
| GTO™ | SuperSOT™-6 | |
| HiSeC™ | SuperSOT™-8 | |

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### Definition of Terms

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|---|---|---|
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