MP2176

6V, 6A, High-Efficiency, Synchronous Step-Down Converter

The Future of Analog IC Technology

DESCRIPTION

The MP2176 is a monolithic, step-down, switch-mode converter with internal power MOSFETs that can achieve up to 6A of continuous output current from a 1.5V to 6V input voltage with excellent load and line regulation. The output voltage can be regulated as low as 0.61V.

Constant-on-time (COT) control provides fast transient response and eases loop stabilization. Fault condition protections include cycle-by-cycle current limiting and thermal shutdown.

The operating frequency is programmed by an external resistor and is compensated for variations in V_{IN}.

Full protection features, including over-current protection (OCP), short-circuit protection (SCP), over-voltage protection (OVP), under-voltage protection (UVP), and over-temperature protection (OTP), are provided by internal comparators.

The MP2176 requires a minimal number of readily available, standard, external components and is available in a QFN-14 (3mmx4mm) package.

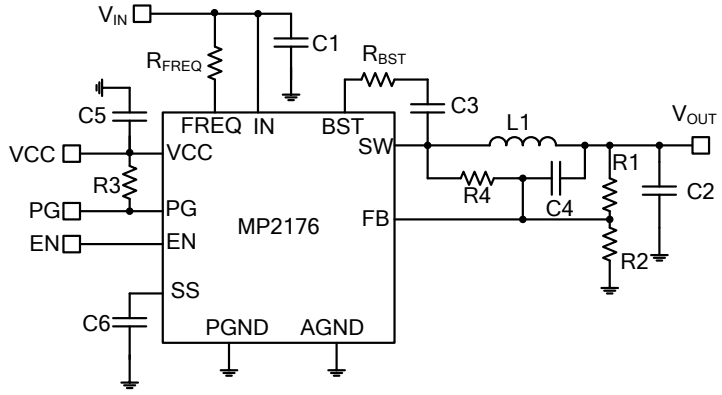
FEATURES

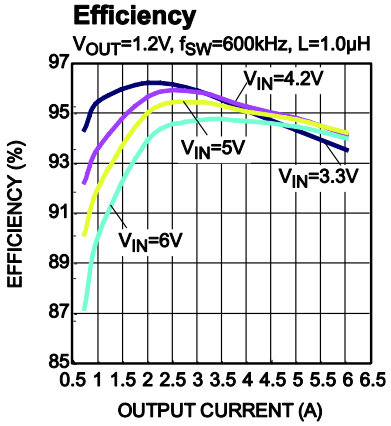
- 1.5V to 6V Wide Input Range
- 3V to 6V VCC Operating Supply
- 6A Output Current
- Programmable Switching Frequency from 300kHz to 1MHz
- Low $R_{DS(ON)}$ Internal Power MOSFETs
- Proprietary Switching Loss Reduction Technique
- 1% Reference Voltage Over -20°C to +85°C Junction Temperature Range
- Pre-Bias Start-Up
- Minimum On Time (T_{ON_MIN} = 60ns) Minimum Off Time (T_{OFF_MIN} = 100ns)
- Non-Latch OCP, Non-Latch OVP, and Thermal Shutdown
- Output Adjustable from 0.61V to 4.5V
- Programmable Soft-Start Time
- Available in a QFN-14 (3mmx4mm) Package

APPLICATIONS

- Flat-Panel Television and Monitors
- Telecom System Base Stations
- Distributed Power Systems
- Personal Video Recorders
- Networking Systems
- Servers

TYPICAL APPLICATION





ORDERING INFORMATION

Part Number*	Package	Top Marking
MP2176GL	QFN-14 (3mmx4mm)	*See Below*

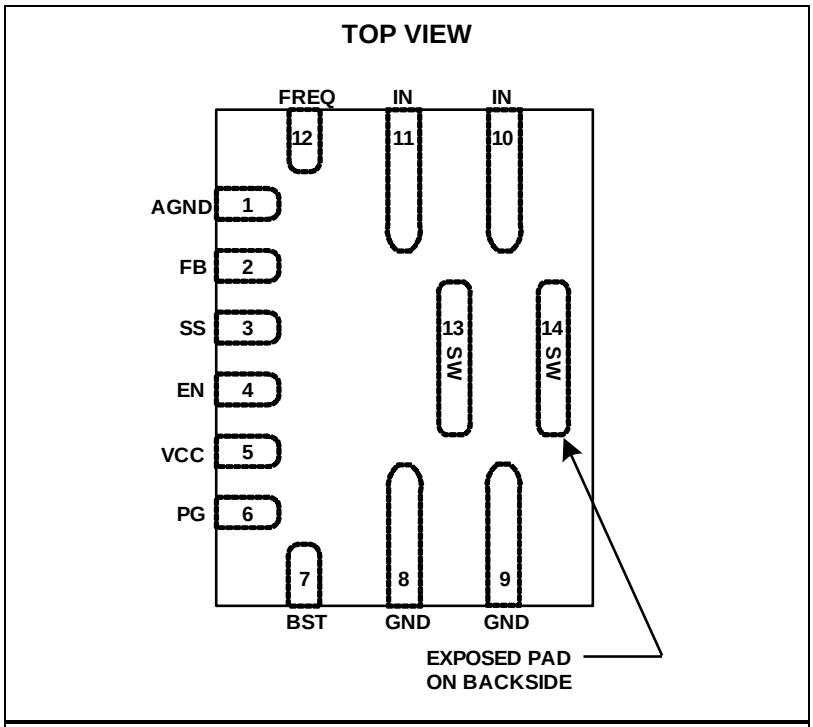
***** For Tape & Reel, add suffix –Z (e.g.: MP2176GL–Z)

TOP MARKING

MPYW
2176
LLL

MP: MPS prefix
Y: Year code
W: Week code
2176: First four digits of the part number
LLL: Lot number

PACKAGE REFERENCE



QFN-14 (3mmx4mm)

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) 6.5V
V_{SW} ..... -0.3V to V_{IN} + 0.3V
V_{SW} (30ns) ..... -3V to V_{IN} + 3V
V_{IN} - V_{SW} ..... -0.3V to V_{IN} + 0.3V
V_{IN} - V_{SW} (30ns) ..... -3V to V_{IN} + 3V
V_{BST} ..... V_{SW} + 6V
All other pins ..... -0.3V to +6V
Continuous power dissipation (T_A = +25°C) (2)
QFN-14 (3mmx4mm) 2.6W
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Storage temperature ..... -65°C to +150°C

Recommended Operating Conditions (3)

Input supply voltage (V_{IN}) ..... 1.5V to 6V
VCC supply voltage (V_{CC}) ..... 3V to 6V
Output voltage (V_{OUT}) ..... 0.61V to 4.5V
Operating junction temp. (T_J). .. -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

	θ_{JA}	θ_{JC}	
QFN-14 (3mmx4mm)	48	10	°C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D(MAX)=(T_J(MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 5V, T_J = -40 to +125°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Supply current (shutdown)	I_{IN}	V_{EN} = 0V		1	2	μA
Supply current (quiescent)	I_{IN}	V_{EN} = 2V, V_{FB} = 1V	0.6	1.05	1.3	mA
High-side switch on resistance	$HS_{RDS(ON)}$	T_J = 25°C		19.8		mΩ
Low-side switch on resistance	$LS_{RDS(ON)}$	T_J = 25°C		15.3		mΩ
Switch leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} = 0V or 5V		0.01	3	μA
High-side current limit	I_{LIMIT}		9.5	12	14.5	A
One-shot on time	t_{ON}	R_{FREQ} = 165kΩ, V_{OUT} = 1.2V		200		ns
Minimum off time	t_{OFF}		50	100	150	ns
Foldback timer (5)	$t_{FOLDBACK}$	OCP occurs		2.5		μs
OVP threshold	V_{OVP}		110%	120%	130%	V
OVP delay (5)	t_{OVP}			1		μs
UVP threshold (5)	V_{UVP}			50%		V_{REF}
Reference voltage	V_{REF}	T_J = -20°C to +85°C	604	610	616	mV
		T_J = -40°C to +125°C	601	610	619	
Feedback current	I_{FB}	V_{FB} = 610mV		0.001	150	nA
Soft-start charging current	I_{SS}	V_{SS} = 0V	5	7.5	10	μA
Enable input low voltage	VILEN		1.4		1.8	V
Enable hysteresis	VEN-HYS			890		mV
Enable input current	I_{EN}	V_{EN} = 2V		1.5	2	μA
		V_{EN} = 0V		0.01	1	
VCC under-voltage lockout threshold rising	VCC_{Vth}		2.3	2.8	2.95	V
VCC under-voltage lockout threshold hysteresis	VCC_{HYS}			300		mV
Power good rising threshold	PG_{Vth-Hi}		84%	90%	96%	V_{REF}
Power good falling threshold	PG_{Vth-Lo}		63%	70%	73%	V_{REF}
Power good deglitch timer	PG_{Td}	T_{SS} = 1ms		2000	5000	μs
Power good sink current capability	V_{PG}	Sink 4mA			0.4	V
Power good leakage current	I_{PG_LEAK}	V_{PG} = 3.3V		50	150	nA
Thermal shutdown (5)	T_{SD}		150	160		°C
Thermal shutdown hysteresis				25		°C

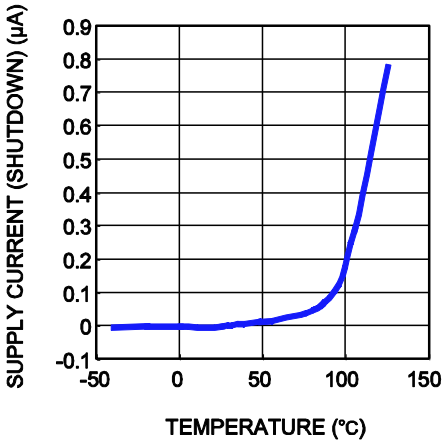
NOTE:

5) Guaranteed by design.

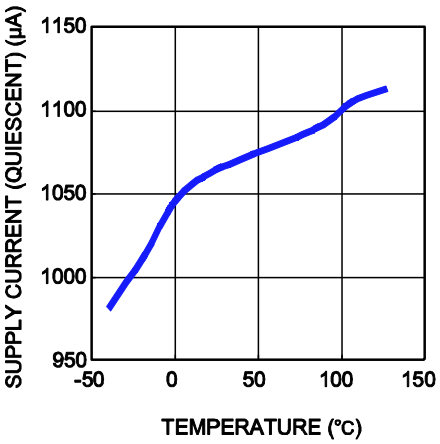
TYPICAL CHARACTERISTICS

Performance waveforms are tested on the evaluation board in the Design Example section.

Supply Current (Shutdown) vs. Temperature

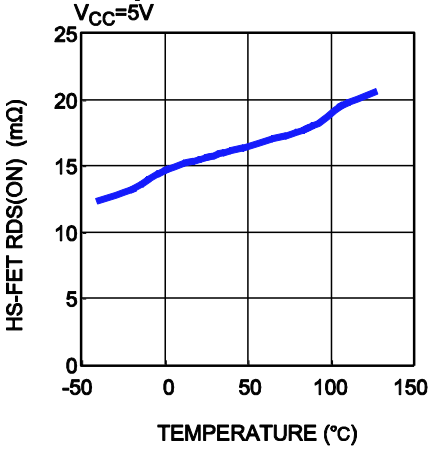


Supply Current (Quiescent) vs. Temperature

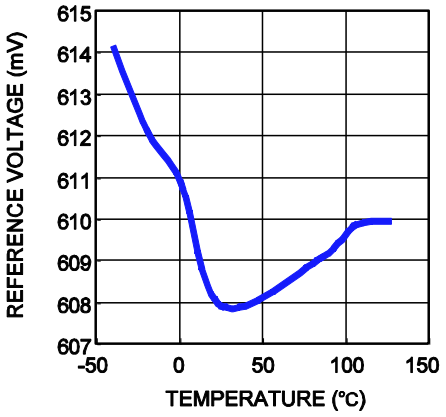


HS-FET $R_{DS(ON)}$ vs. Temperature

V_{CC}=5V

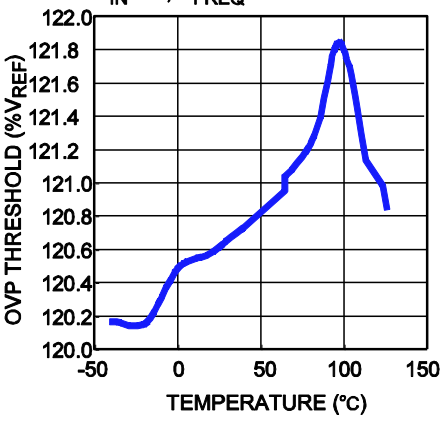


Reference Voltage vs. Temperature



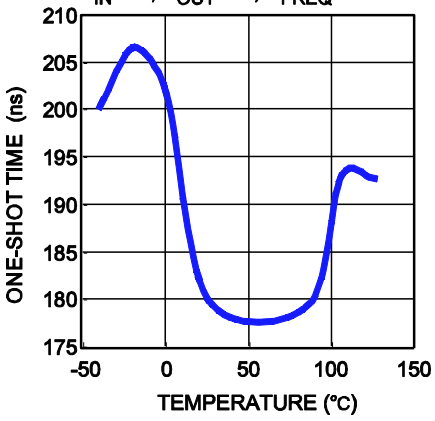
OVP Threshold vs. Temperature

V_{IN}=5V, R_{FREQ}=100kΩ



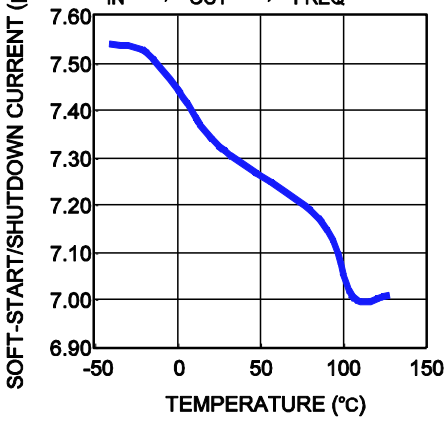
One-Shot Time vs. Temperature

V_{IN}=5V, V_{OUT}=1V, R_{FREQ}=165kΩ

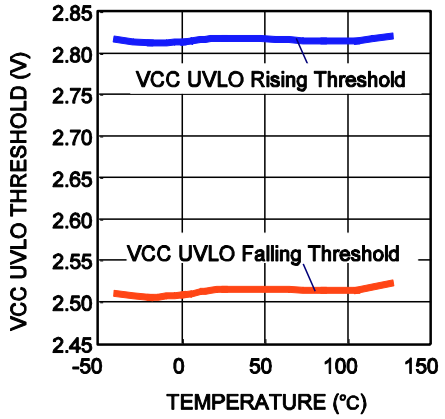


Soft-Start/Shutdown Current vs. Temperature

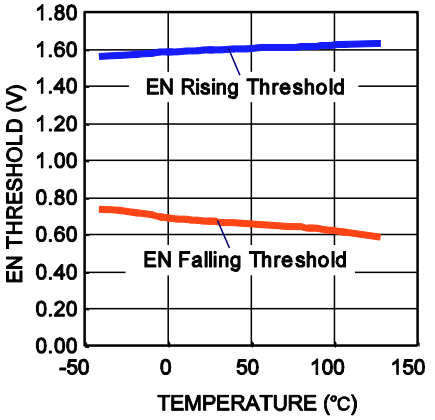
V_{IN}=5V, V_{OUT}=1V, R_{FREQ}=165kΩ



VCC UVLO Threshold vs. Temperature



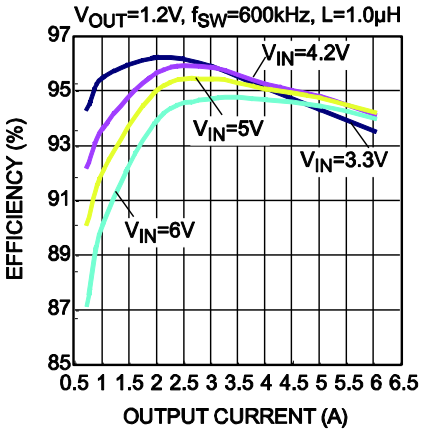
EN Threshold vs. Temperature



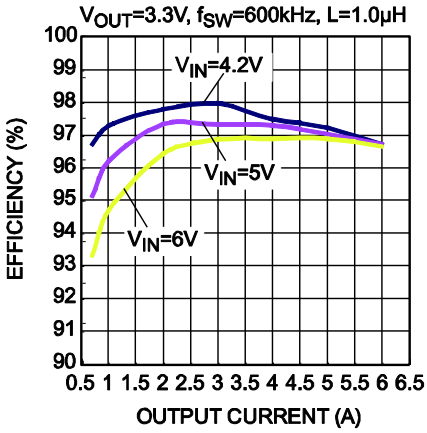
TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested on the evaluation board in the Design Example section. V_{IN} = 5V, V_{OUT} = 1.2V, L = 1.0µH, T_A = +25°C, unless otherwise noted.

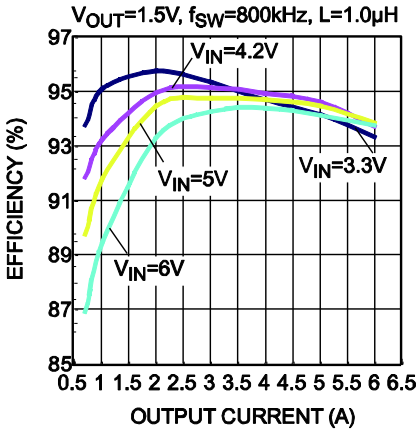
Efficiency



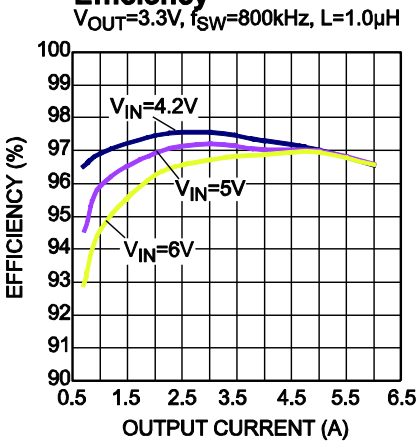
Efficiency



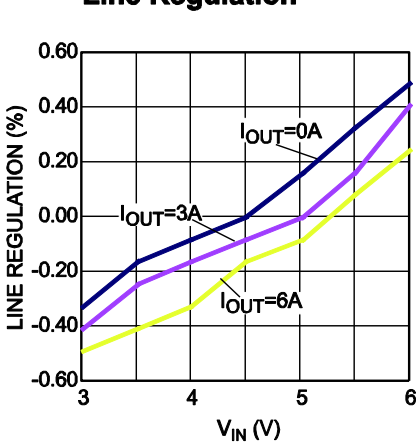
Efficiency



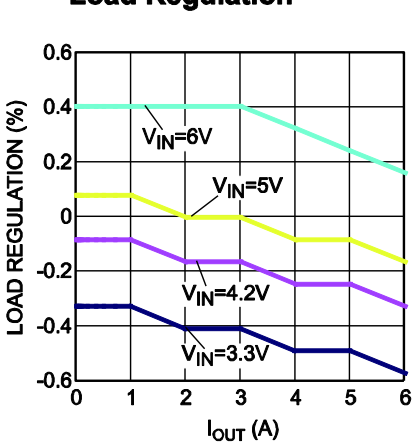
Efficiency



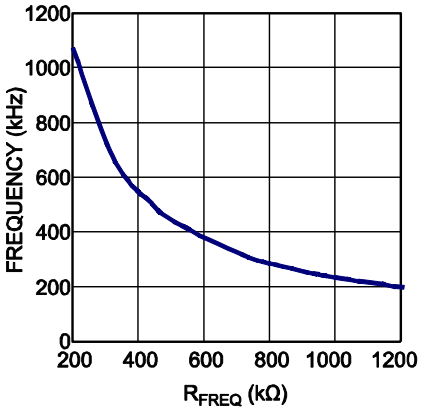
Line Regulation



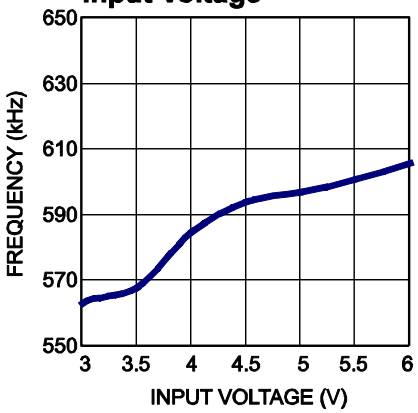
Load Regulation



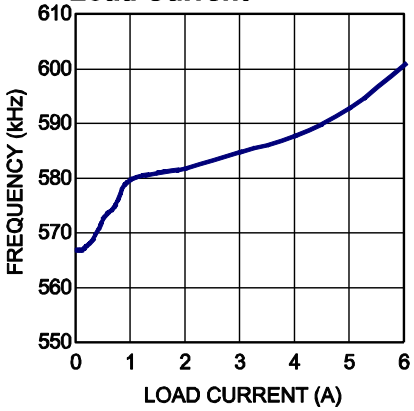
Frequency vs. R_{FREQ}



Frequency vs. Input Voltage



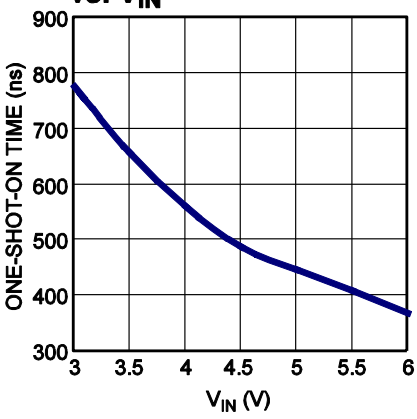
Frequency vs. Load Current



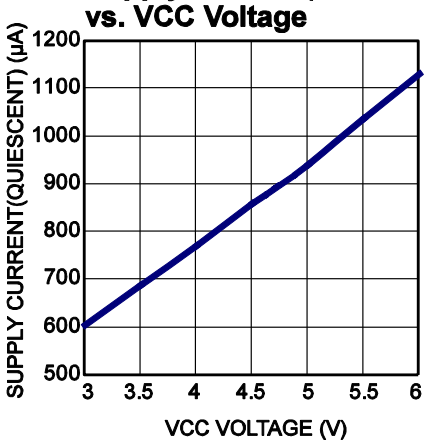
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board in the Design Example section. V_{IN} = 5V, V_{OUT} = 1.2V, L = 1.0µH, T_A = +25°C, unless otherwise noted.

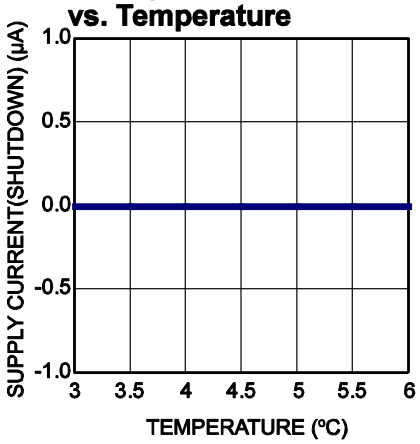
One-Shot On Time vs. V_{IN}



Supply Current (Quiescent) vs. VCC Voltage



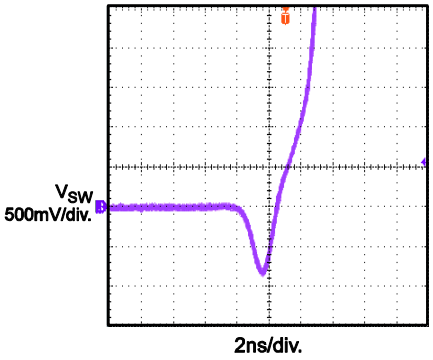
Supply Current (Shutdown) vs. Temperature



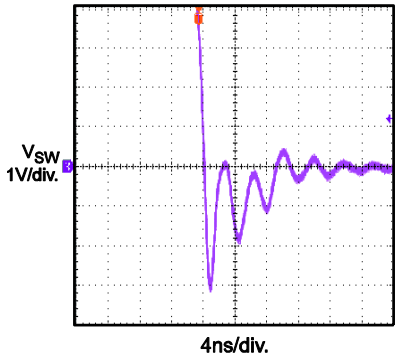
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board in the Design Example section. V_{IN} = 5V, V_{OUT} = 1.2V, L = 1.0µH, T_A = +25°C, unless otherwise noted.

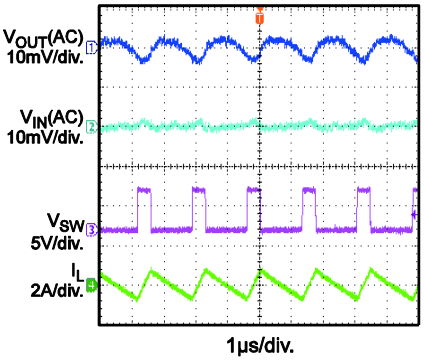
Dead Time (on)
I_{OUT} = 6A



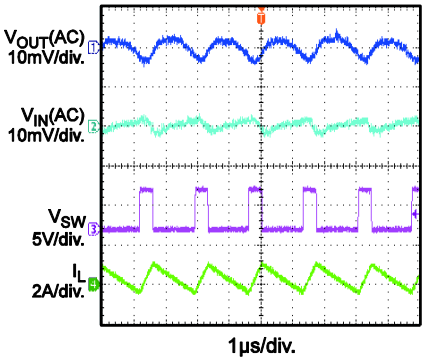
Dead Time (off)
I_{OUT} = 6A



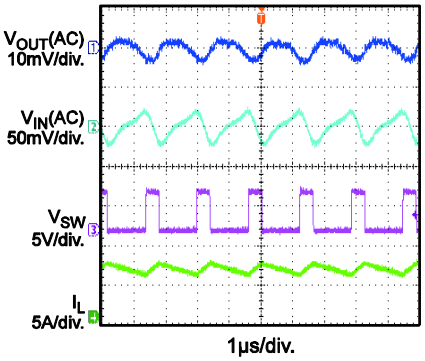
Input/Output Voltage Ripple
I_{OUT} = 0A



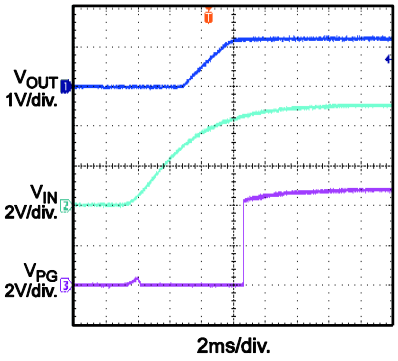
Input/Output Voltage Ripple
I_{OUT} = 0.3A



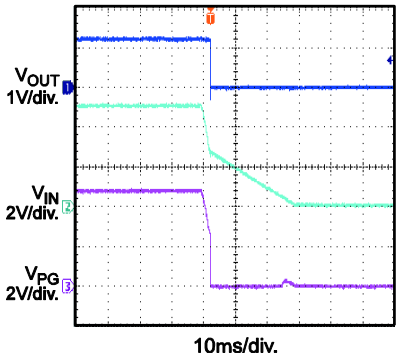
Input/Output Voltage Ripple
I_{OUT} = 6A



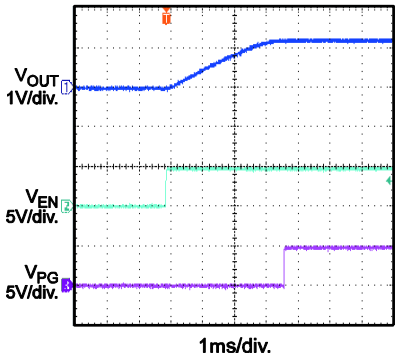
Power Good through V_{IN} Start-Up
I_{OUT} = 6A



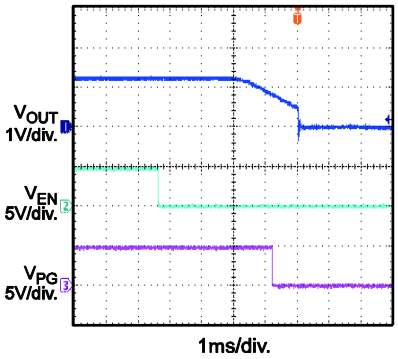
Power Good through V_{IN} Shutdown
I_{OUT} = 6A



Power Good through EN Start-Up
I_{OUT} = 6A



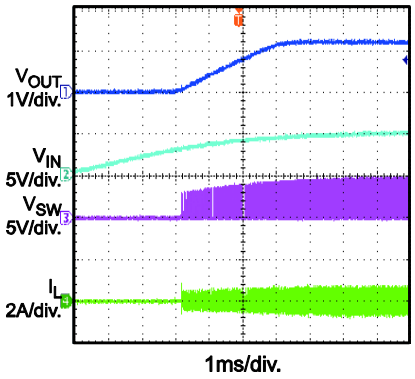
Power Good through EN Shutdown
I_{OUT} = 6A



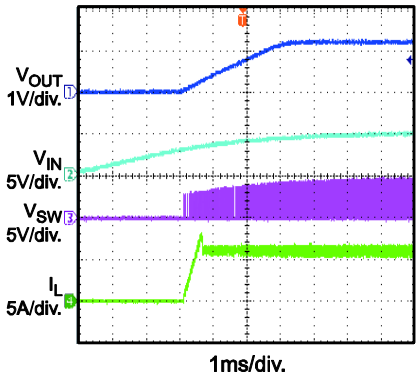
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board in the Design Example section. V_{IN} = 5V, V_{OUT} = 1.2V, L = 1.0µH, T_A = +25°C, unless otherwise noted.

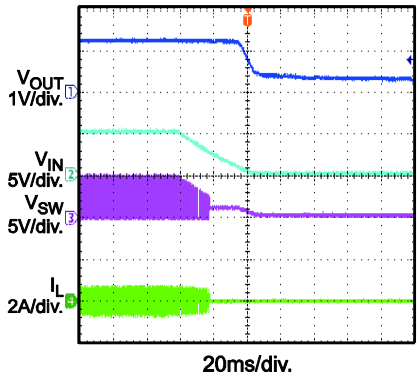
Start-Up through V_{IN}
I_{OUT} = 0A



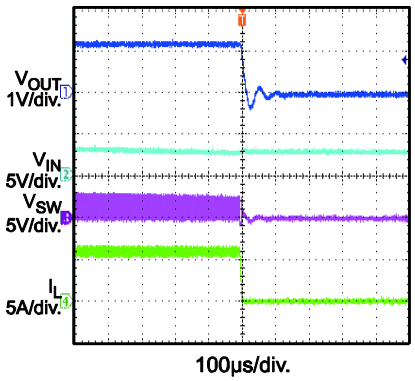
Start-Up through V_{IN}
I_{OUT} = 6A



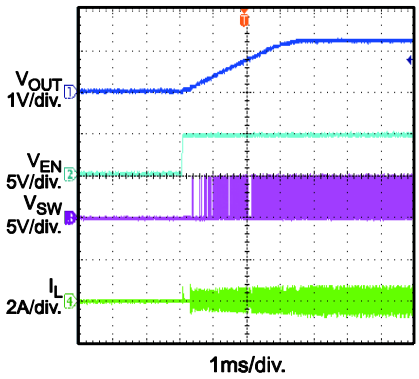
Shutdown through V_{IN}
I_{OUT} = 0A



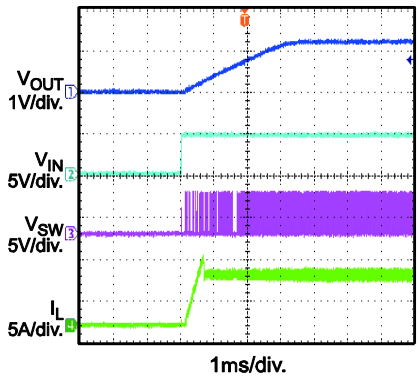
Shutdown through V_{IN}
I_{OUT} = 6A



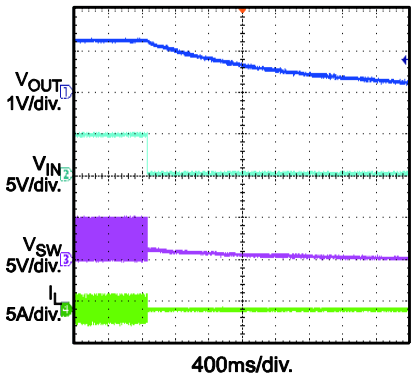
Start-Up through EN
I_{OUT} = 0A



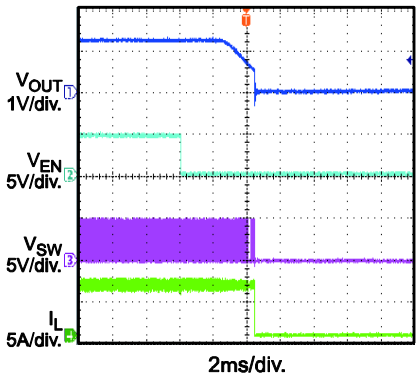
Start-Up through EN
I_{OUT} = 6A



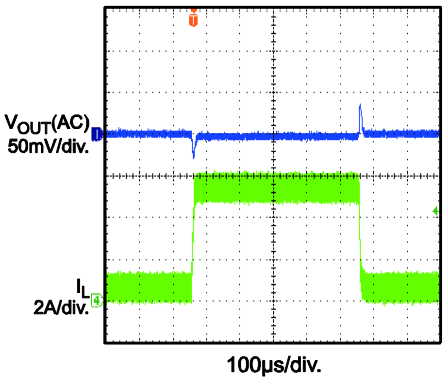
Shutdown through EN
I_{OUT} = 0A



Shutdown through EN
I_{OUT} = 6A



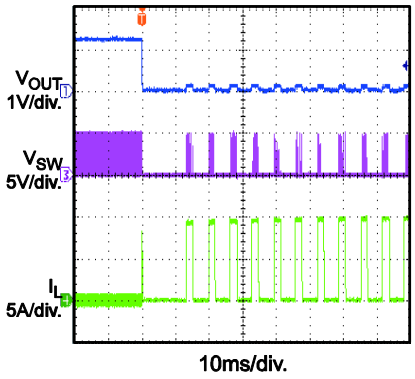
Transient
I_{OUT} = 0.6A-5.4A@2.5A/µs,
f_{SW} = 600kHz, C_{OUT} = 4x22µF



TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

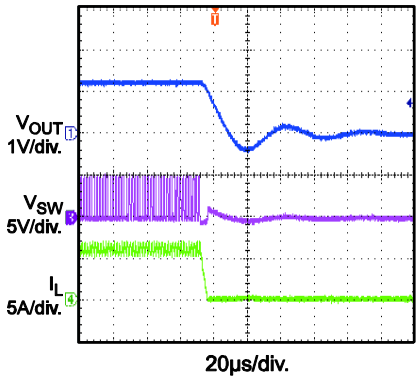
Performance waveforms are tested on the evaluation board in the Design Example section. V_{IN} = 5V, V_{OUT} = 1.2V, L = 1.0µH, T_A = +25°C, unless otherwise noted.

Short-Circuit Protection



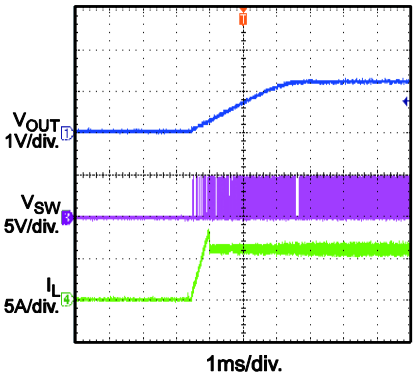
Thermal Shutdown

I_{OUT} = 6A



Thermal Recovery

I_{OUT} = 6A



PIN FUNCTIONS

PIN #	Name	Description
1	AGND	**Analog ground.**
2	FB	**Feedback.** The output voltage is set by an external resistor divider from the output to GND tapped to FB. The resistor divider should be placed as close to FB as possible. Avoid placing vias on the FB traces.
3	SS	**Soft start.** Connect an external capacitor to SS to program the soft-start time for the switch-mode regulator.
4	EN	**Enable.** Pull EN higher than 1.8V to enable the chip. For automatic start-up, connect EN to V_{IN} with a 100kΩ resistor. EN can be used to set the on/off threshold (adjust UVLO) with two additional resistors.
5	VCC	**External bias supply voltage for the driver and control circuits.** For 1.5V to 3V input applications, provide VCC with a separate 3.3V/5V bias supply. For 3V to 6V input applications, provide VCC with a separate 3.3V/5V bias supply or tie VCC to V_{IN} with a 10Ω resistor. Decouple VCC with a minimum 4.7μF ceramic capacitor placed as close to VCC as possible. X7R or X5R grade dielectric ceramic capacitors are recommended for their stable temperature characteristics.
6	PG	**Power good output.** PG is high if the output voltage is higher than 90% of the nominal voltage. There is a delay from the time FB becomes greater than or equal to 90% to when PG goes high.
7	BST	**Bootstrap.** A capacitor connected between SW and BST is required to form a floating supply across the high-side switch driver.
8 - 9	GND	**System ground.** GND is the reference ground of the regulated output voltage. For this reason, care must be taken during the PCB layout.
10 - 11	IN	**Supply voltage.** IN supplies power for the internal MOSFET and regulator. The MP2176 operates from a +3V to +6V input rail. An input capacitor is needed to decouple the input rail. Use wide PCB traces and multiple vias to make the connection.
12	FREQ	**Frequency setting.** A resistor connected between FREQ and IN is required to set the switching frequency. The on time is determined by the input voltage and the resistor connected to FREQ. IN connected through a resistor is used for line feed-forward and makes the frequency constant during the input voltage's variation. It is recommend to use a 10pF decoupling capacitor from FREQ to GND.
13 - 14	SW	**Switch output.** Connect SW to the inductor and bootstrap capacitor. SW is driven up to V_{IN} by the high-side switch during the on time of the PWM duty cycle. The inductor current drives SW negative during the off time. The on resistance of the low-side switch and the internal Schottky diode fixes the negative voltage. Use wide PCB traces to make the connection.

BLOCK DIAGRAM

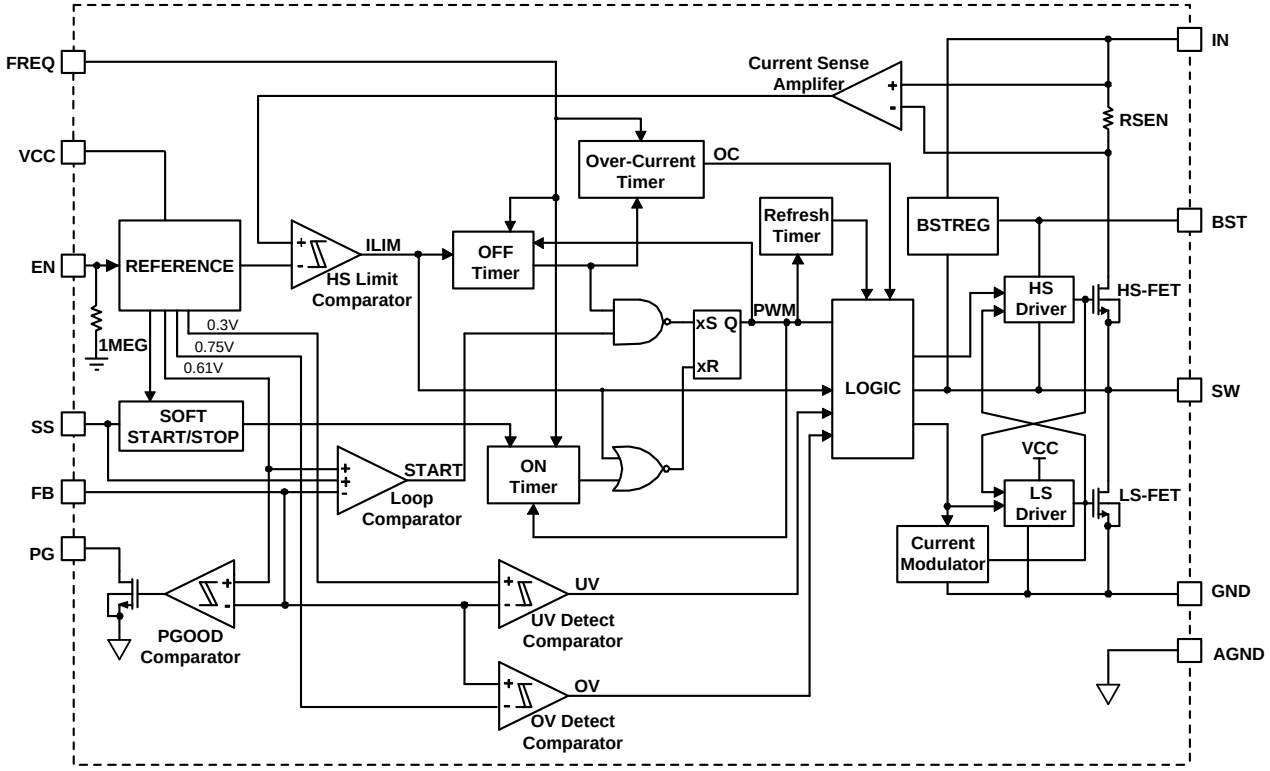


Figure 1: Functional Block Diagram

OPERATION

Pulse-Width Modulation (PWM) Operation

The MP2176 is a fully integrated, synchronous, rectified, step-down, switch-mode converter. Constant-on-time (COT) control is employed to provide fast transient response and ease loop stabilization. At the beginning of each cycle, the high-side MOSFET (HS-FET) is turned on when the feedback voltage (V_{FB}) is below the reference voltage (V_{REF}), which indicates an insufficient output voltage. The on period is determined by the input voltage, and the frequency-set resistor is determined with Equation (1):

$$t_{ON}(ns) = \frac{4.8 \times R_{FREQ}(k\Omega)}{V_{IN}(V) - 0.49} \quad (1)$$

After the on period elapses, the HS-FET is turned off. The HS-FET is turned on again when V_{FB} drops below V_{REF}. By repeating operation in this way, the converter regulates the output voltage. The integrated low-side MOSFET (LS-FET) is turned on when the HS-FET is in its off state to minimize conduction loss. There is a dead short between the input and GND if both the HS-FET and LS-FET are turned on at the same time. This is called shoot-through. To avoid shoot-through, a dead time (DT) is generated internally between the HS-FET off and LS-FET on period or the LS-FET off and HS-FET on period.

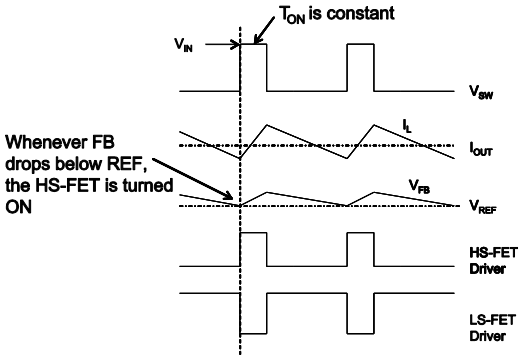


Figure 2: PWM Operation

The MP2176 always operates in continuous conduction mode (CCM), which means that the inductor current can go negative in light-load operation (see Figure 2). When V_{FB} is below V_{REF}, the HS-FET is turned on for a fixed interval determined by the one-shot on-timer. When the HS-FET is turned off, the LS-MOSFET is turned on until the next period begins. When the MP2176 operates in CCM, the switching frequency is fairly constant. This is called pulse-width modulation (PWM) mode.

Switching Frequency

Selecting the switching frequency is a trade-off between efficiency and component size. Low-frequency operation increases efficiency by reducing MOSFET switching losses, but requires a larger inductance and capacitance to maintain a low output voltage ripple.

For the MP2176, the on time can be set using FREQ. In this way, the frequency is set in steady-state operation in CCM.

Adaptive COT control is used in the MP2176, and there is no dedicated oscillator in the IC. Connect FREQ to IN through a resistor (R_{FREQ}), and the input voltage is forward fed to the one-shot on-time timer through R_{FREQ}. In steady-state operation at CCM, the duty ratio is kept as V_{OUT}/V_{IN}. Therefore, the switching frequency is fairly constant over the input voltage range. The switching frequency can be set with Equation (2):

$$f_{SW}(kHz) = \frac{10^6}{\frac{4.8 \times R_{FREQ}(k\Omega)}{V_{IN}(V) - 0.49} \times \frac{V_{IN}(V)}{V_{OUT}(V)} + t_{DELAY}(ns)} \quad (2)$$

Where t_{DELAY} is the comparator delay (about 40ns).

Generally, the MP2176 is set for 300kHz - 1MHz applications and is optimized to operate at a high switching frequency with high efficiency. With a high switching frequency, small LC filter components can be used to save system PCB space.

Jitter and FB Ramp Slope

Figure 3 shows jitter occurring in PWM mode. When there is noise in the V_{FB} downward slope, the on time of the HS-FET deviates from its intended location and produces jitter. Note that there is a relationship between a system's stability and the steepness of the V_{FB} ripple's downward slope. The slope steepness of the V_{FB} ripple dominates in noise immunity. The magnitude of the V_{FB} ripple does affect noise immunity directly.

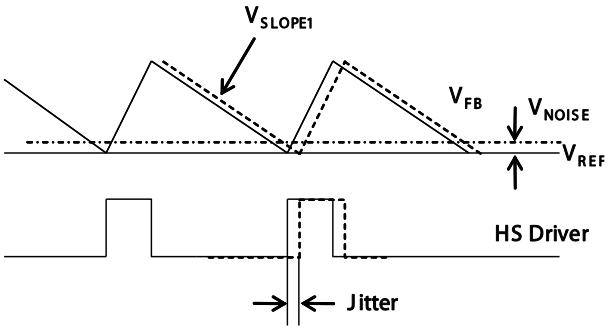


Figure 3: Jitter in PWM Mode

Ramp with Large ESR Capacitor

When POSCAPs or other types of capacitors with large ESR are applied as output capacitors, the ESR ripple dominates the output ripple, and the slope on FB is related to the ESR. Figure 4 shows an equivalent circuit in PWM mode with the HS-FET off and without an external ramp circuit. Refer to the Application Information section on page 17 for design steps using large ESR capacitors.

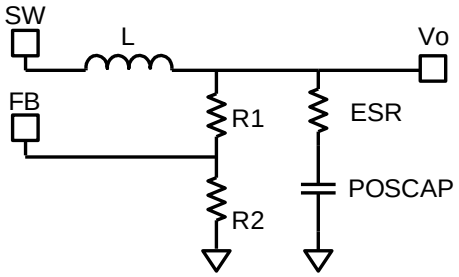


Figure 4: Simplified Circuit in PWM Mode without External Ramp Compensation

To achieve stability when no external ramp is applied, calculate the ESR value with Equation (3):

$$R_{ESR} \geq \frac{\frac{t_{SW}}{0.7\times\pi}+\frac{t_{ON}}{2}}{C_{OUT}} \quad (3)$$

Where T_{SW} is the switching period.

Ramp with Small ESR Capacitor

When the output capacitors are ceramic, the ESR ripple is not high enough to stabilize the system, and external ramp compensation is required. Refer to the Application Information section on page 17 for design steps using small ESR capacitors.

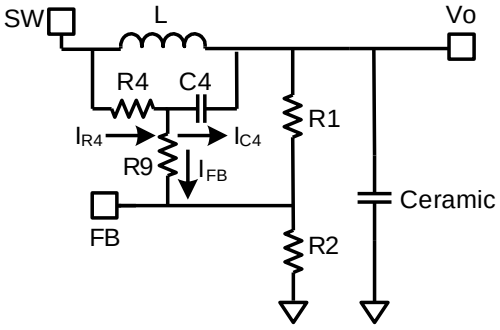


Figure 5: Simplified Circuit in PWM Mode with External Ramp Compensation

Figure 5 shows a simplified equivalent circuit with the HS-FET off and using an external ramp compensation circuit (R4, C4) in PWM mode. The external ramp is derived from the inductor ripple current. Calculate C4, R9, R1, and R2 with Equation (4):

$$\frac{1}{2\pi\times f_{SW}\times C_4} < \frac{1}{20}\times\left(\frac{R_1\times R_2}{R_1+R_2}+R_9\right) \quad (4)$$

The current of R4 can be calculated with Equation (5):

$$I_{R4} = I_{C4} + I_{FB} \approx I_{C4} \quad (5)$$

The ramp on V_{FB} can then be estimated with Equation (6):

$$V_{RAMP} = \frac{V_{IN}-V_O}{R_4\times C_4}\times t_{ON}\times\left(\frac{R_1 // R_2}{R_1 // R_2 + R_9}\right) \quad (6)$$

The downward slope of the V_{FB} ripple can then be calculated with Equation (7):

$$V_{SLOPE1} = \frac{V_{RAMP}}{t_{off}} = \frac{-V_{OUT}}{R_4\times C_4} \quad (7)$$

As shown in Equation (7), if there is instability in PWM mode, either R4 or C4 can be reduced. If C4 cannot be reduced further due to limitations from Equation (4), then only R4 can be reduced. For stable PWM operation, V_{slope1} should be designed following Equation (8):

$$-V_{SLOPE1} \geq \frac{\frac{t_{SW}}{0.7\times\pi}+\frac{t_{ON}}{2}-R_{ESR}\times C_{OUT}}{2\times L\times C_{OUT}}\times V_{OUT}+\frac{0.7\times I_O\times 10^{-3}}{t_{sw}-t_{on}} \quad (8)$$

Where I_O is the load current.

Over-Current Protection (OCP)

The MP2176 enters over-current protection (OCP) mode when the inductor current reaches the current limit and attempts to recover from the over-current fault with hiccup mode. In OCP, the chip disables the output power stage, discharges the soft-start capacitor, and then attempts to soft-start again automatically. If the over-current condition still remains after the soft start ends, the chip repeats this operation cycle until the over-current condition is removed and the output rises back to the regulation level. The MP2176 also operates in hiccup mode when a short circuit occurs.

Power Good (PG)

The MP2176 has a power-good (PG) output that can be connected to V_{CC} or another voltage source through a resistor (e.g.: 100kΩ). When the MP2176 is powered on, and V_{FB} is above 90% of V_{REF}, PG is pulled high.

When V_{FB} drops to 70% of V_{REF} or the part is not powered on, PG is pulled low.

Soft Start/Stop (SS)

The MP2176 employs a soft-start/-stop (SS) mechanism to ensure a smooth output during power-up and power-down.

When EN rises high, an internal current source (8μA) charges up the SS capacitor (C6). The SS capacitor voltage takes over V_{REF} to the PWM comparator. The output voltage ramps up smoothly with the SS voltage (V_{SS}). Once V_{SS} reaches the same level as V_{REF}, V_{SS} continues ramping up while V_{REF} takes over the PWM comparator. At this point, the soft start finishes, and the device enters steady-state operation.

When EN is pulled low, the SS cap voltage is discharged through an 8μA internal current source. Once V_{SS} reaches V_{REF}, it takes over the PWM comparator. The output voltage decreases smoothly with V_{SS} until it reaches zero. The SS capacitor value can be determined with Equation (9):

$$C_{SS}(nF) = \frac{t_{SS}(ms) \times I_{SS}(\mu A)}{V_{REF}} \quad (9)$$

If the output capacitors have a large capacitance value, the SS time should not be too small. Otherwise, the current limit can be reached easily during SS. A minimum value of 4.7nF should be used if the output capacitance value is larger than 330μF.

Over-/Under-Voltage Protection (OVP/UVP)

The MP2176 has non-latching over-voltage protection (OVP). The device monitors the output voltage through a resistor divider V_{FB} to detect an over-voltage condition on the output. When V_{FB} is higher than 120% of V_{REF} (0.610V), the LS-FET is turned on while the HS-FET is off. The LS-FET remains on until it reaches the negative current limit and turns off for 100ns. If the over-voltage condition still remains, the chip repeats this operation cycle until V_{FB} drops below 110% of V_{REF}.

When V_{FB} is below 50% of V_{REF} (0.610V), this is recognized as an under-voltage (UV) condition. Usually, under-voltage protection (UVP) is caused by an over-current (OC) condition and results in over-current protection (OCP).

Configuring the EN Control

EN provides an electrical on/off control of the device. Drive EN high to turn on the regulator. Drive EN low to turn off the regulator. Do not float EN.

For automatic start-up, EN can be pulled up to the input voltage through a resistive voltage divider. Determine the automatic start-up voltage by choosing the values of the pull-up resistor (R_{UP} from IN to EN) and the pull-down resistor (R_{DOWN} from EN to GND) with Equation (10):

$$V_{IN-START} = 1.4 \times \frac{R_{UP} + R_{DOWN}}{R_{DOWN}} \quad (10)$$

For example, when R_{UP} = 100kΩ and R_{DOWN} = 51kΩ, $V_{IN-START}$ is 4.15V.

To prevent noise, use a 10nF ceramic capacitor from EN to GND.

Pre-Bias Start-Up

If the output is pre-biased to a certain voltage during start-up, the MP2176 disables the switching of both the high-side and low-side switches until the voltage on the internal soft-

start capacitor exceeds the sensed output voltage at FB. There is an internal Zener diode on EN, which clamps the EN voltage to prevent a runaway. Assuming a worst-case 6V internal Zener clamp, the maximum pull-up current should be less than 1mA. Therefore, when EN is driven by an external logic signal, the EN voltage should be lower than 6V. When EN is connected to IN through a pull-up resistor or a resistive voltage divider, the resistance selection should ensure that the maximum pull-up current is less than 1mA.

If using a resistive voltage divider and an IN value higher than 6V, the allowed minimum pull-up resistor (R_{UP}) should meet Equation (11):

$$\frac{V_{IN}(V)-6}{R_{UP}(k\Omega)}-\frac{6}{R_{DOWN}(k\Omega)}<1(mA) \quad (11)$$

As a result, when only R_{UP} is applied, $V_{IN\text{-}START}$ is determined by the input under-voltage lockout (UVLO). The value of R_{UP} can be calculated with Equation (12):

$$R_{UP}(k\Omega)>\frac{V_{IN}(V)-6}{1(mA)} \quad (12)$$

A typical pull-up resistor is 100kΩ.

Thermal Shutdown

Thermal shutdown is employed in the MP2176. The junction temperature of the IC is monitored internally. If the junction temperature exceeds the threshold value (minimum 150°C), the converter shuts off. This is a non-latch protection. There is a hysteresis of about 25°C. Once the junction temperature drops to about 125°C, a soft start-up is initiated.

Under-Voltage Lockout (UVLO) Protection

The MP2176 has a UVLO protection. When VCC is higher than the UVLO rising threshold voltage, the MP2176 is powered up. The MP2176 shuts off when VCC is lower than the UVLO falling threshold voltage. This is a non-latch protection.

The MP2176 is disabled when VCC falls below its UVLO falling threshold (2.45V). If an application requires a higher UVLO, use EN to adjust the input voltage UVLO by using two external resistors (see Figure 6). It is recommended to use the EN resistors to set the UVLO falling threshold (V_{STOP}) above 2.8V. The rising threshold (V_{START}) should be set to provide enough of a hysteresis to allow for any input supply variation.

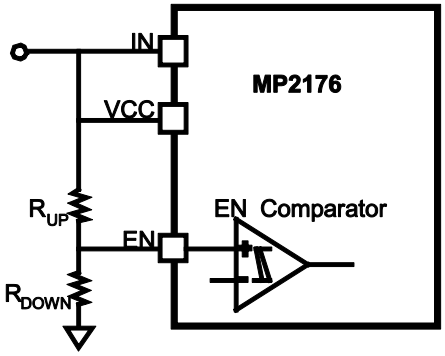


Figure 6: Adjustable UVLO

APPLICATION INFORMATION

Setting the Output Voltage with Large ESR Capacitors

For applications that use electrolytic capacitors or POSCAPs with a controlled ERS output as output capacitors, the output voltage is set by feedback resistors R1 and R2 (see Figure 7).

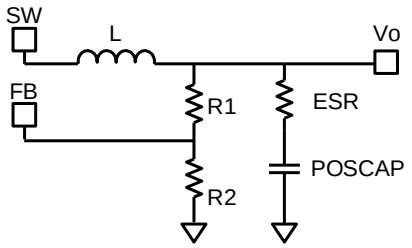


Figure 7: Simplified POSCAP Circuit

First, choose a value for R2. R2 should be chosen reasonably, since a small R2 leads to considerable quiescent current loss, but a large R2 makes FB noise-sensitive. R2 should be between 5 - 100kΩ. Use a comparatively larger R2 when V_{OUT} is low and a smaller R2 when V_{OUT} is high. Considering the output ripple, determine R1 with Equation (13):

$$R_1 = \frac{V_{OUT} - \frac{1}{2} \times \Delta V_{OUT} - V_{REF}}{V_{REF}} \times R_2 \quad (13)$$

Where ΔV_{OUT} is the output ripple determined in Equation (22).

Setting the Output Voltage with Small ESR Capacitors

When low ESR ceramic capacitors are used in the output, an external voltage ramp should be added to FB through a resistor (R4) and capacitor (C4). The output voltage is influenced by the ramp voltage (V_{RAMP}) in addition to a resistor divider (see Figure 8).

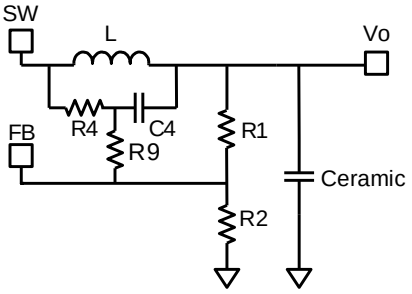


Figure 8: Simplified Ceramic Capacitor Circuit

V_{RAMP} can be calculated with Equation (6). R2 should be chosen reasonably, since a small R2 leads to considerable quiescent current loss, but a large R2 makes FB noise-sensitive. R2 should be between 5 - 100kΩ. Use a comparatively larger R2 when V_{OUT} is low and a smaller R2 when V_{OUT} is high. Then the value of R1 can be determined with Equation (14):

$$R_1 = \frac{R_2}{\frac{V_{FB(AVG)}}{V_{OUT} - V_{FB(AVG)}} - \frac{R_2}{R_4 + R_9}} \quad (14)$$

Where $V_{FB(AVG)}$ is the average value on FB. The value of $V_{FB(AVG)}$ varies with V_{IN}, V_{OUT}, and the load condition, meaning the load regulation is strictly related to $V_{FB(AVG)}$. The line regulation is related to $V_{FB(AVG)}$, as well. For better load or line regulation, use a lower V_{RAMP} once it meets Equation (8).

For PWM operation, $V_{FB(AVG)}$ can be calculated with Equation (15):

$$V_{FB(AVG)} = V_{REF} + \frac{1}{2} \times V_{RAMP} \times \frac{R_1 // R_2}{R_1 // R_2 + R_9} \quad (15)$$

Usually, R9 is set to 0Ω. R9 should be five times smaller than R1//R2 to minimize its influence on Vramp. To achieve better noise immunity, R9 can also be set using Equation (16):

$$R_9 \le \frac{1}{10} \times \frac{R_1 \times R_2}{R_1 + R_2} \quad (16)$$

Using Equation (14) and Equation (15) to calculate the output voltage can be complicated. To simplify the calculation of R1 in Equation (14), add a DC-blocking capacitor (Cdc) to filter the DC influence from R4 and R9. Figure 9 shows a simplified circuit with external ramp compensation and a Cdc. With this capacitor, R1 can calculated easily for PWM mode operation with Equation (17):

$$R_1 = \frac{V_{OUT} - V_{REF} - \frac{1}{2} \times V_{RAMP}}{V_{REF} + \frac{1}{2} \times V_{RAMP}} \times R_2 \quad (17)$$

Cdc is suggested to be at least 10 times larger than C4 for better DC blocking performance. Cdc should be no larger than 0.47μF, considering the start-up performance. For better FB noise immunity, combine a larger Cdc with a reduced R1 and R2 to limit the Cdc to a reasonable value without affecting system start-up. Note that even when the Cdc is applied, the load and line regulation are still related to V_{RAMP}.

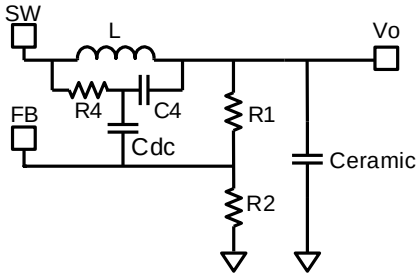


Figure 9: Simplified Circuit of a Ceramic Capacitor with a DC Blocking Capacitor

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous and therefore requires a capacitor to supply AC current to the step-down converter while maintaining the DC input voltage. Ceramic capacitors are recommended for the best performance. In the layout, place the input capacitors as close to IN as possible.

The capacitance varies significantly with the temperature. Capacitors with X5R and X7R ceramic dielectrics are recommended because they are fairly stable over-temperature.

The capacitors must also have a ripple current rating greater than the maximum input ripple current of the converter. The input ripple current can be estimated with Equation (18):

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (18)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, shown in Equation (19):

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (19)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitance value determines the input voltage ripple of the converter. If there is an input voltage ripple requirement in the system design, choose an input capacitor that meets the specification The input voltage ripple can be estimated with Equation (20):

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (20)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, shown in Equation (21):

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{f_{SW} \times C_{IN}} \quad (21)$$

Selecting the Output Capacitor

The output capacitor is required to maintain the DC output voltage. Ceramic or POSCAP capacitors are recommended. The output voltage ripple can be estimated with Equation (22):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}) \quad (22)$$

In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is caused mainly by the capacitance. For simplification, the output voltage ripple can be estimated with Equation (23):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (23)$$

The output voltage ripple caused by the ESR is very small and therefore requires an external ramp to stabilize the system. The external ramp can be generated through a resistor (R4) and capacitor (C4) following Equation (4), Equation (7), and Equation (8).

In the case of POSCAP capacitors, the ESR dominates the impedance at the switching frequency. The ramp voltage generated from the ESR is high enough to stabilize the system and therefore does not require an external ramp. A minimum ESR value (calculated with Equation (3)) is required to ensure stable operation of the converter.

For simplification, the output ripple can be approximated with Equation (24):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (24)$$

Selecting the Inductor

An inductor is required to supply constant current to the output load while being driven by the switching input voltage. A larger-value inductor results in less ripple current and lower output ripple voltage but also has a larger physical size, higher series resistance, and lower saturation current. A good rule for determining the inductor value is to allow the peak-to-peak ripple current in the inductor to be approximately 10 ~ 30% of the maximum output current. Also, ensure that the peak inductor current is below the current limit of the device. The inductance value can be calculated with Equation (25):

$$L = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (25)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

Choose an inductor that will not saturate under the maximum inductor peak current. The peak inductor current can be calculated with Equation (26):

$$I_{LP} = I_{OUT} + \frac{V_{OUT}}{2 \times f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (26)$$

The inductors listed in Table 1 are highly recommended for the high efficiency they can provide.

Typical Design Parameter Tables

The tables on page 20 include recommended component values for typical output voltages (1.0V, 1.2V, 1.8V, 3.3V) and switching frequencies (600kHz, 800kHz, 1MHz). Refer to Table 2 and Table 3 for design cases without external ramp compensation. Refer to Table 4 and Table 5 for design cases with external ramp compensation. An external ramp is not required when high ESR capacitors, such as electrolytic or POSCAPs, are used. An external ramp is required when low ESR capacitors, such as ceramic capacitors, are used. For cases not listed in this datasheet, a calculator in an Excel spreadsheet can also be requested through an MPS sales representative to assist with the calculation.

Table 1: Inductor Selection Guide

Part Number	Manufacturer	Inductance (µH)	DCR (mΩ)	Current Rating (A)	Dimensions L x W x H (mm^3)	Switching Frequency (kHz)
FDU1250C-R50M	TOKO	0.50	1.3	46.3	13.3 x 12.1 x 5	1000
FDU1250C-R56M	TOKO	0.56	1.6	42.6	13.3 x 12.1 x 5	800 - 1000
FDU1250C-R75M	TOKO	0.75	1.7	32.7	13.3 x 12.1 x 5	600 - 800
FDU1250C-1R0M	TOKO	1.0	2.2	31.3	13.3 x 12.1 x 5	600

Table 2: C_{OUT} POSCAP, 600kHz, $5V_{IN}$

V_{OUT} (V)	L (µH)	R1 (kΩ)	R2 (kΩ)	R7 (kΩ)
1.0	1.0	19.8	30	300
1.2	1.0	29.4	30	365
1.5	1.0	29.4	20	453
1.8	1.0	39.2	20	549
3.3	1.0	44.2	10	1000

Table 3: C_{OUT} POSCAP, 800kHz, $5V_{IN}$

V_{OUT} (V)	L (µH)	R1 (kΩ)	R2 (kΩ)	R7 (kΩ)
1.0	0.75	20	30	210
1.2	0.75	20	20	270
1.5	0.75	30	20	330
1.8	0.75	39	20	499
3.3	0.75	44.2	10	750

Table 4: C_{OUT} Ceramic, 600kHz, $5V_{IN}$

V_{OUT} (V)	L (µH)	R1 (kΩ)	R2 (kΩ)	R4 (kΩ)	C4 (pF)	R7 (kΩ)
1.0	1.0	21	30	240	470	309
1.2	1.0	33	30	220	470	365
1.5	1.0	51	30	330	390	464
1.8	1.0	45	20	270	470	549
3.3	1.0	62	10	160	680	953

Table 5: C_{OUT} Ceramic, 800kHz, $5V_{IN}$

V_{OUT} (V)	L (µH)	R1 (kΩ)	R2 (kΩ)	R4 (kΩ)	C4 (pF)	R7 (kΩ)
1.0	0.75	21	30	200	470	226
1.2	0.75	34	30	200	470	270
1.5	0.75	34	20	220	470	324
1.8	0.75	47.5	20	225	470	402
3.3	0.75	57.6	10	200	560	750

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. A four-layer layout is strongly recommended to achieve better thermal performance. For best results, refer to Figure 10 and Figure 11 and follow the guidelines below.

1. Place at least nine vias (10/20mil hole/diameter size) just beneath the IC for the best decoupling effect.
2. Place 10 or more vias (10/25mil hole/diameter size) each for the input and GND copper next to IN and PGND to improve the thermal performance.
3. Place a 22µF (1206/1210) input capacitor (C1B) on the bottom layer just beneath the VIN and PGND vias for the best input decoupling effect.
4. If VIN/PGND vias are not allowed beneath the IC: Place a 22µF input capacitor with a 1206/1210 package (C1C) is required on the top layer, connecting to the VIN and PGND copper directly (within 2mm of the IC edge).
5. Place a solid PGND layer on the first inner layer just below the IC layer.
6. Keep the high-current paths (GND, IN, and SW) very close to the device with short, direct, and wide traces.
7. Place the VCC decoupling capacitor (C5) as close to VCC as possible.
8. Connect the VCC GND net to the PGND copper.
9. Connect all AGND signals together to AGND.
10. Kelvin-connect AGND to PGND near the C5 GND pad on the top layer.
11. Keep the AGND trace 20mil or wider.
12. Place the external feedback resistors next to FB.
13. Ensure that there is no via on the FB trace.
14. Keep the vias away from the switching node (SW).
15. Keep the BST voltage path (BST, C3, R_{BST}, and SW) as short as possible.
16. Keep the V_{OUT} sense trace away from noise signals (SW, VIN, etc).
17. Place the V_{OUT} sense point at a stable, quiet output point close to the V_{OUT} capacitor.

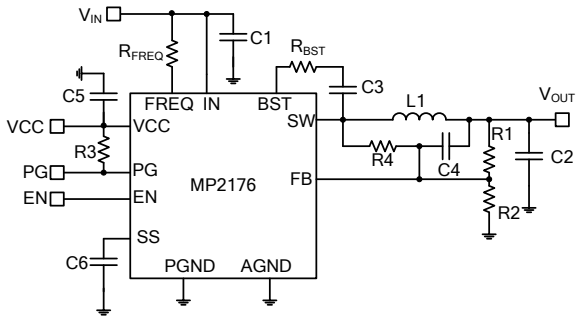


Figure 10: Schematic for PCB Layout Guidelines

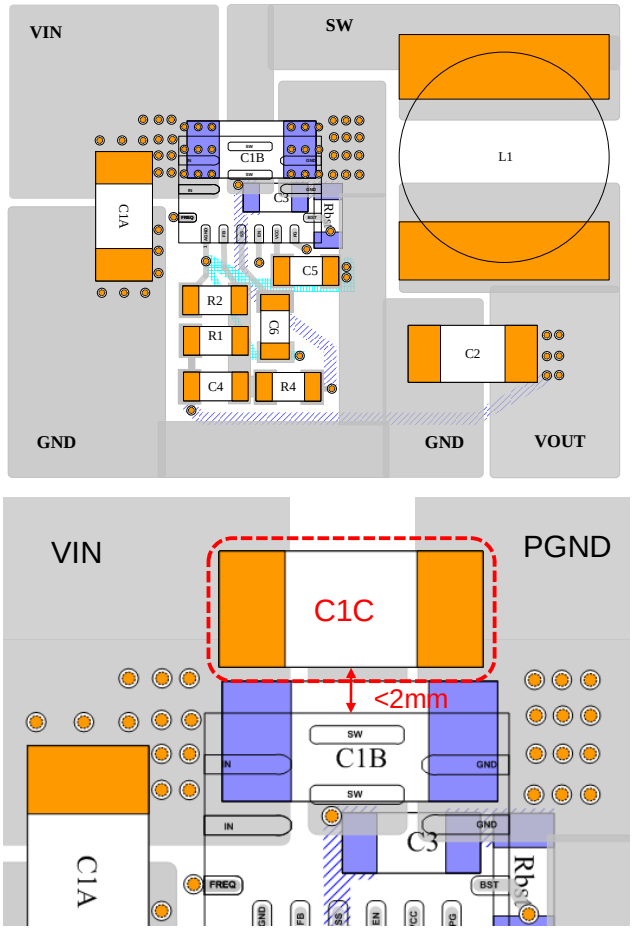


Figure 11: Recommended Layout

TYPICAL APPLICATION CIRCUIT

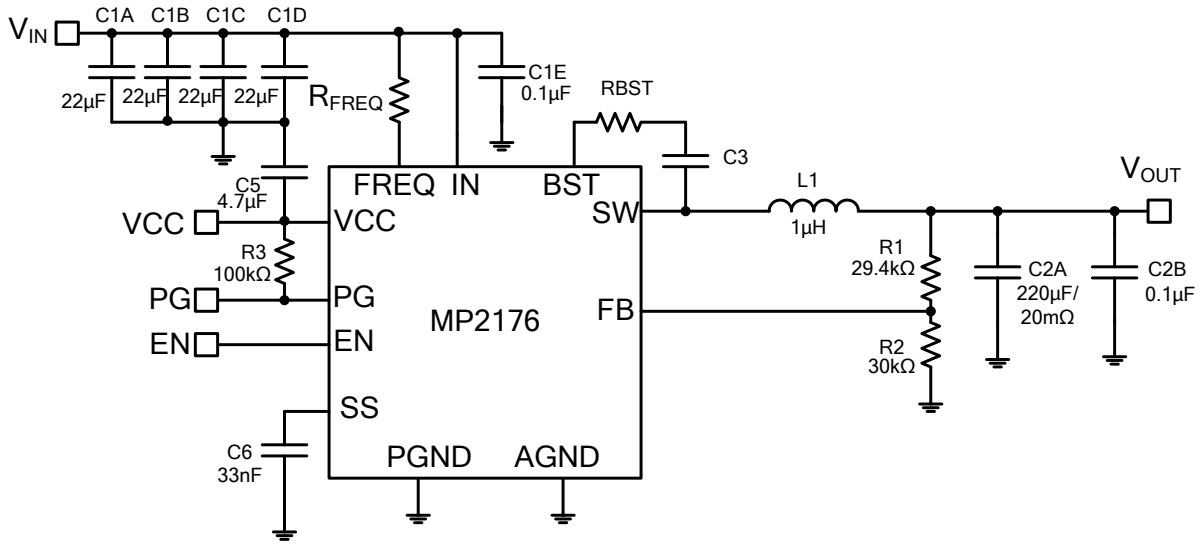
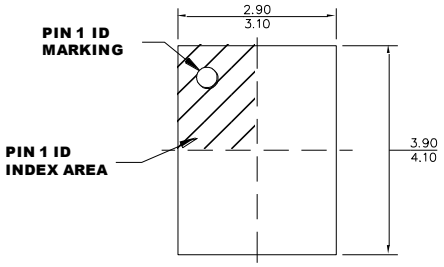


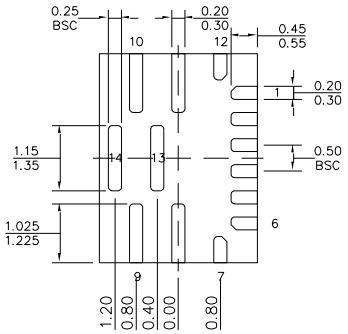
Figure 13: Typical Application Circuit with No External Ramp, V_{IN} = 5V, V_{OUT} = 1.2V, I_{OUT} = 6A, f_{SW} = 600kHz

PACKAGE INFORMATION

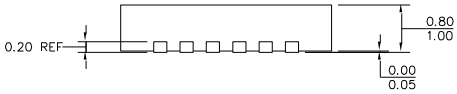
QFN-14 (3mmx4mm)



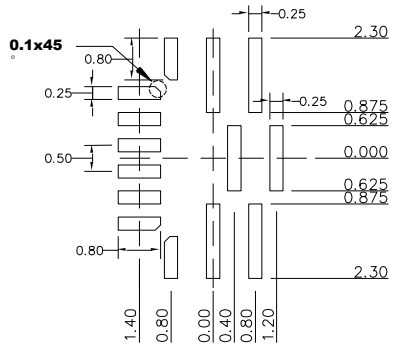
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.