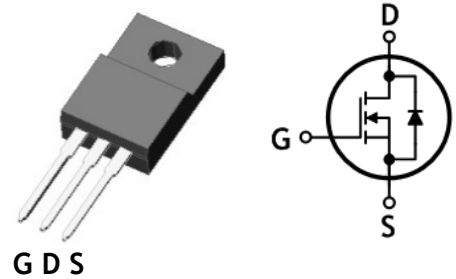


N-Channel Super Junction MOSFET

Features

- Drain-Source voltage: $V_{DS}=700V$ (@ $T_J=150^\circ C$)
- Low drain-source On resistance: $R_{DS(on)}=0.38\Omega$ (Max.)
- Ultra low gate charge: $Q_g=20nC$ (Typ.)
- RoHS compliant device
- 100% avalanche tested

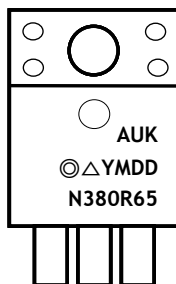


Ordering Information

Part Number	Marking	Package
SJMN380R65AF	N380R65	TO-220F-3L

TO-220F-3L

Marking Information



Column 1: Manufacturer
 Column 2: Production Information
 e.g.) ©△YMDD
 -. ©△: Factory Management Code
 -. YMDD: Date Code (Year, Month, Daily)
 Column 3: Device Code

Absolute maximum ratings ($T_C=25^\circ C$ unless otherwise noted)

Characteristic	Symbol	Rating	Unit	
Drain-source voltage	V_{DSS}	650	V	
Gate-source voltage	V_{GSS}	± 30	V	
Drain current (DC) (Note 1)	I_D	$T_C=25^\circ C$	11	A
		$T_C=100^\circ C$	7	A
Drain current (Pulsed) (Note 1)	I_{DM}	44	A	
Single pulsed avalanche energy (Note 2)	E_{AS}	135	mJ	
Repetitive avalanche current (Note 1)	I_{AR}	5	A	
Repetitive avalanche energy (Note 1)	E_{AR}	63.2	mJ	
Power dissipation	P_D	32	W	
Diode dv/dt ruggedness (Note 3)	dv/dt	15	V/ns	
MOSFET dv/dt ruggedness (Note 4)	dv/dt	50	V/ns	
Junction temperature	T_J	150	$^\circ C$	
Storage temperature range	T_{stg}	-55-150	$^\circ C$	

Thermal Characteristics

Characteristic	Symbol	Rating	Unit
Thermal resistance, junction to case	$R_{th(j-c)}$	Max. 3.9	°C/W
Thermal resistance, junction to ambient	$R_{th(j-a)}$	Max. 62.5	

Electrical Characteristics ($T_C=25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Drain-source breakdown voltage	BV_{DSS}	$I_D=250\mu\text{A}$, $V_{GS}=0$	650	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$I_D=250\mu\text{A}$, $V_{DS}=V_{GS}$	2	3	4	V
Drain-source cut-off current	I_{DSS}	$V_{DS}=650\text{V}$, $V_{GS}=0\text{V}$	-	-	1	μA
		$V_{DS}=650\text{V}$, $T_J=125^\circ\text{C}$	-	-	100	μA
Gate leakage current	I_{GSS}	$V_{DS}=0\text{V}$, $V_{GS}=\pm 30\text{V}$	-	-	± 100	nA
Drain-source on-resistance	$R_{DS(ON)}$	$V_{GS}=10\text{V}$, $I_D=5.5\text{A}$	-	0.31	0.38	Ω
Internal gate resistance	R_g	$f=1\text{MHz}$, Open drain	-	21	28	Ω
Input capacitance	C_{iss}	$V_{DS}=25\text{V}$, $V_{GS}=0\text{V}$, $f=1\text{MHz}$	629	787	945	pF
Output capacitance	C_{oss}		344	431	518	
Reverse transfer capacitance	C_{rss}		19	24	29	
Turn-on delay time (Note 3)	$t_{d(on)}$	$V_{DS}=350\text{V}$, $I_D=11\text{A}$, $R_G=25\Omega$	-	17	25	ns
Rise time (Note 3)	t_r		-	14	24	
Turn-off delay time (Note 3)	$t_{d(off)}$		-	40	55	
Fall time (Note 3)	t_f		-	5	8	
Total gate charge (Note 4)	Q_g	$V_{DS}=400\text{V}$, $V_{GS}=10\text{V}$, $I_D=7\text{A}$	-	20	25	nC
Gate-source charge (Note 4)	Q_{gs}		-	6.5	10	
Gate-drain charge (Note 4)	Q_{gd}		-	5	10	

Source-Drain Diode Ratings and Characteristics ($T_C=25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Source current (DC)	I_S	Integral reverse diode in the MOSFET	-	-	11	A
Source current (Pulsed)	I_{SM}		-	-	44	A
Forward voltage	V_{SD}	$V_{GS}=0\text{V}$, $I_S=11\text{A}$	-	-	1.2	V
Reverse recovery time (Note 3,4)	t_{rr}	$I_S=11\text{A}$, $V_{GS}=0\text{V}$, $dI_S/dt=100\text{A}/\mu\text{s}$	-	326	450	ns
Reverse recovery charge (Note 3,4)	Q_{rr}		-	2.8	4.5	μC

Note:

1. Calculated continuous current based on maximum allowable junction temperature
2. $L=10\text{mH}$, $I_{AS}=5\text{A}$, $V_{DD}=50\text{V}$, Starting $T_J=25^\circ\text{C}$
3. Guaranteed by design, not subject to production testing
4. Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$

Typical Electrical Characteristics Curves

Fig. 1 Typical Output Characteristics

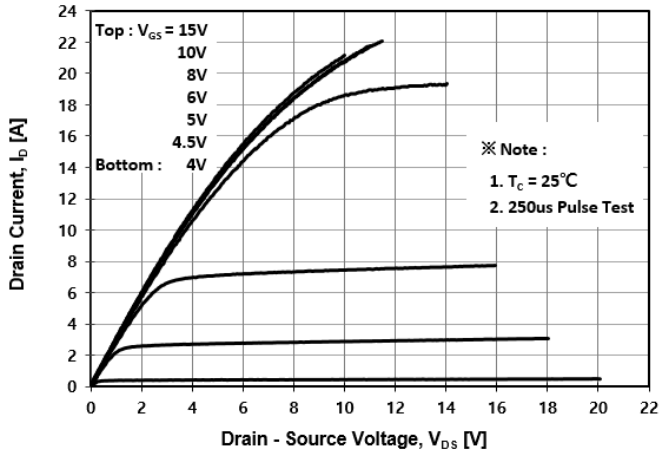


Fig. 2 Typical Transfer Characteristics

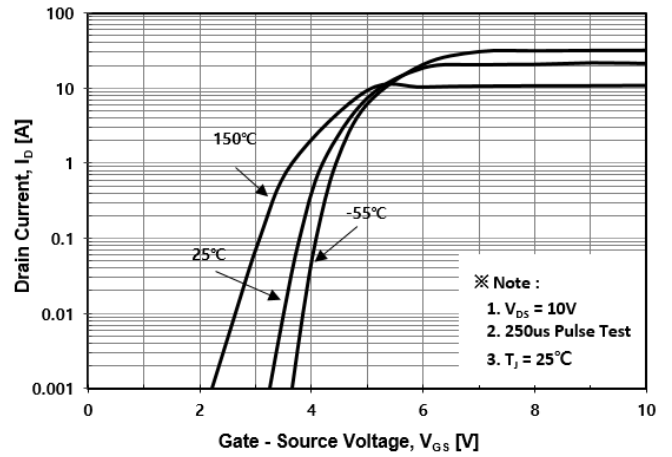


Fig.3 On-Resistance Variation with Drain Current and Gate Voltage

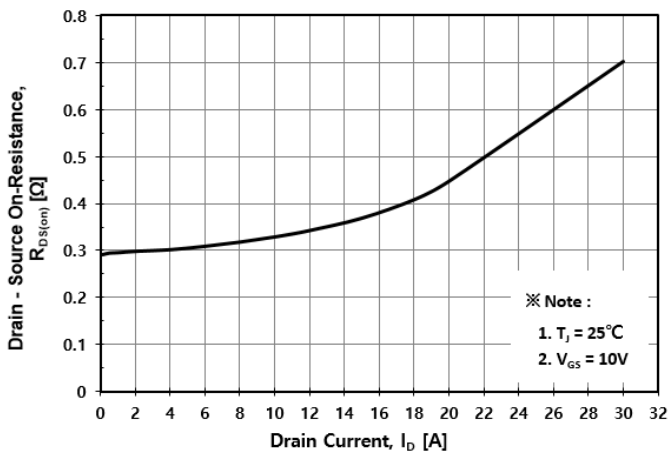


Fig. 4 Body Diode Forward Voltage Variation with Source Current

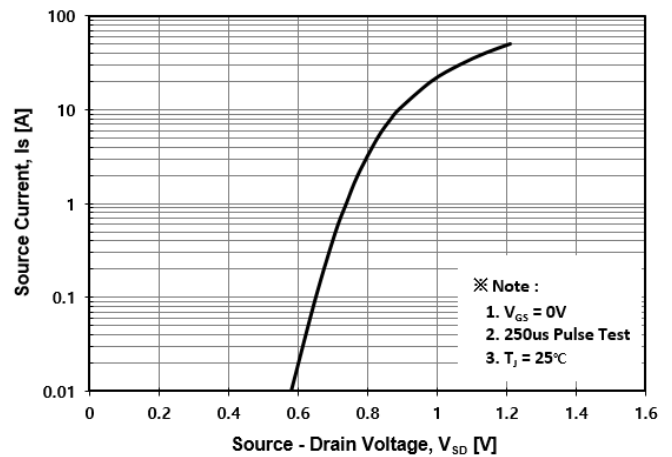


Fig. 5 Typical Capacitance Characteristics

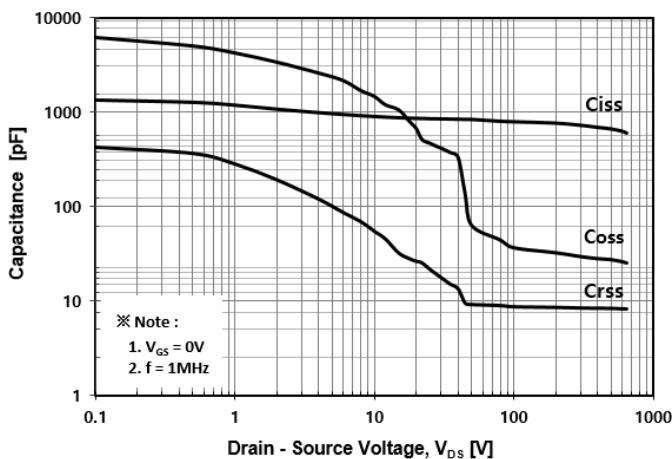


Fig. 6 Typical Total Gate Charge Characteristics

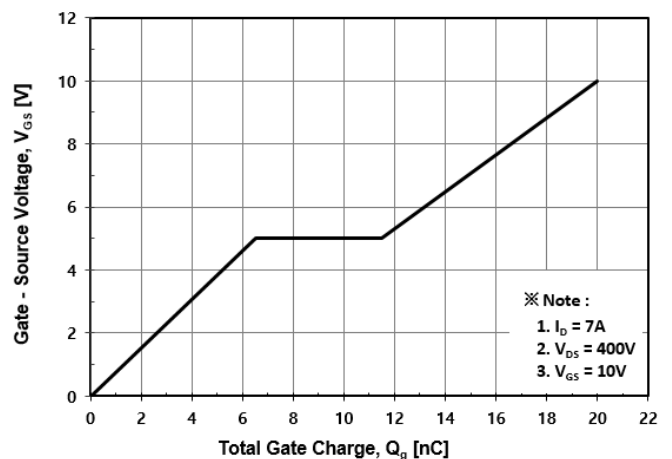


Fig. 7 Breakdown Voltage Variation vs. Temperature

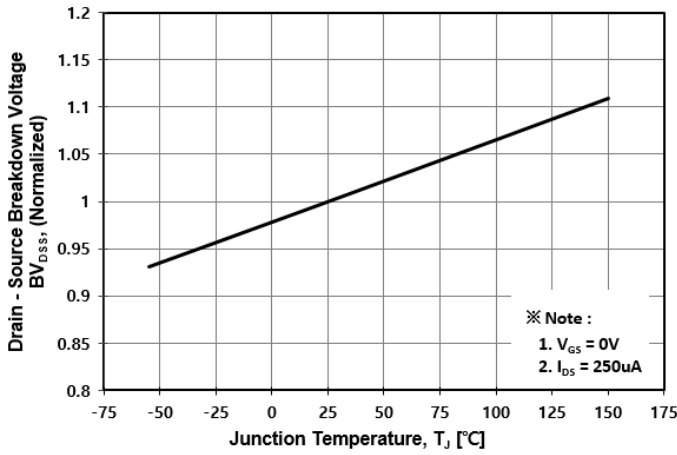


Fig. 8 On-Resistance Variation vs. Temperature

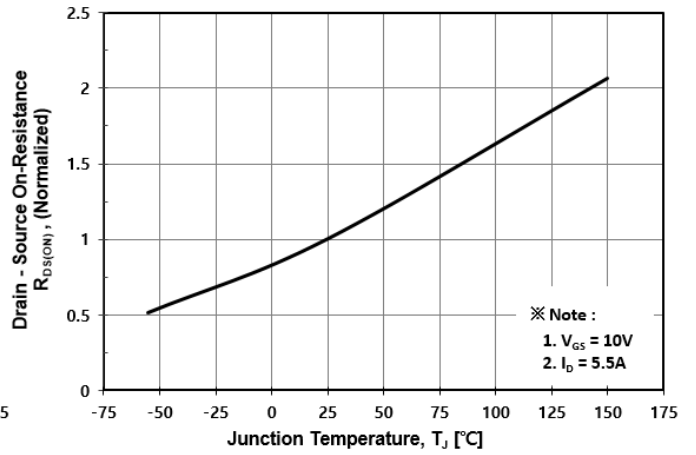


Fig. 9 Maximum Drain Current vs. Case Temperature

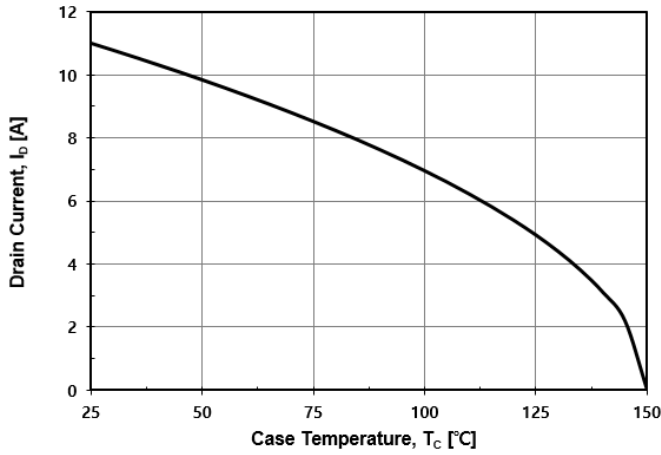


Fig. 10 Maximum Safe Operating Area

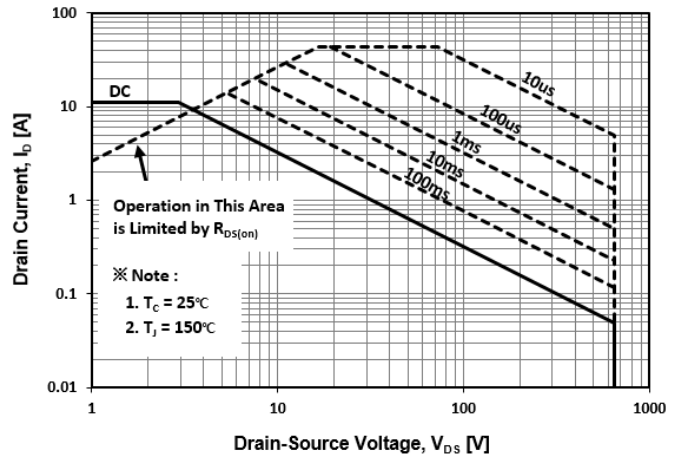


Fig. 11 Transient Thermal Impedance

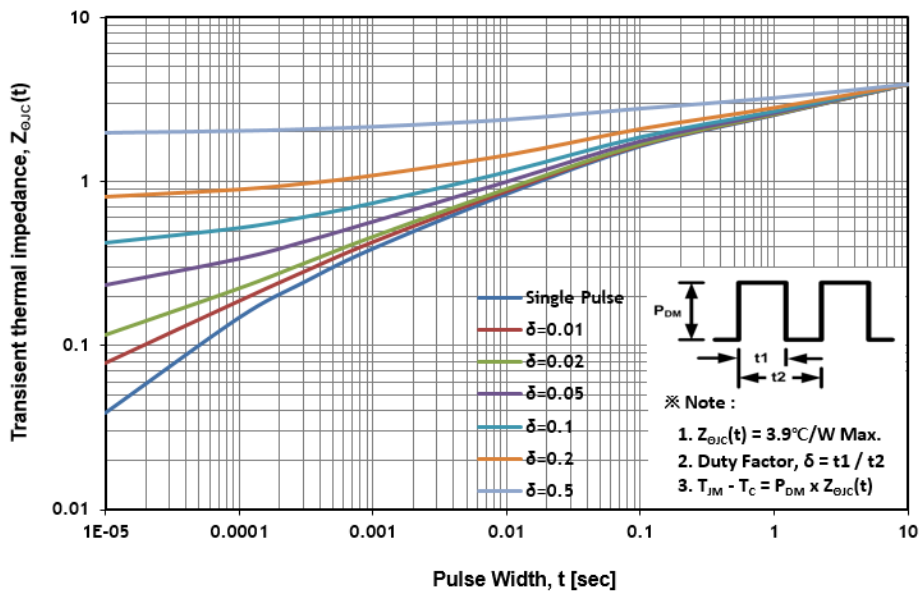


Fig. 12 Gate Charge Test Circuit & Waveform

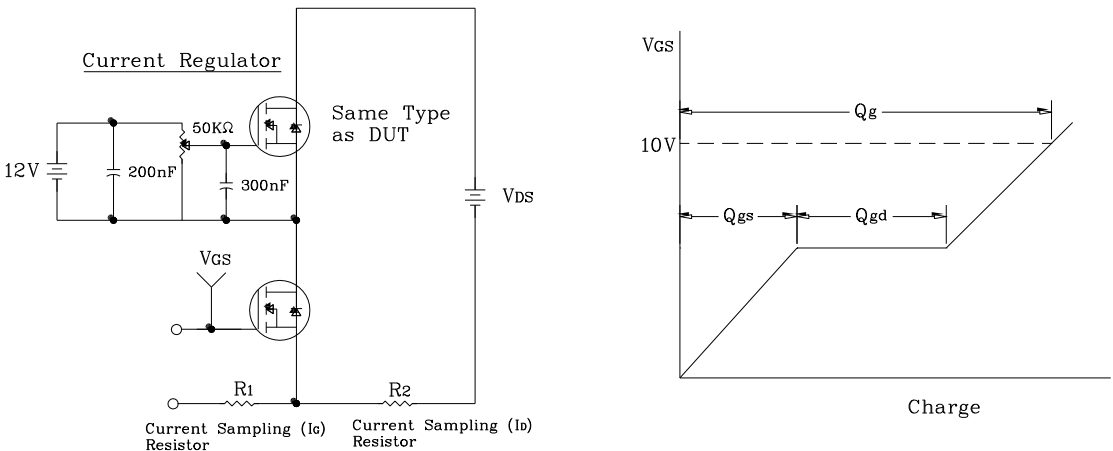


Fig. 13 Resistive Switching Test Circuit & Waveform

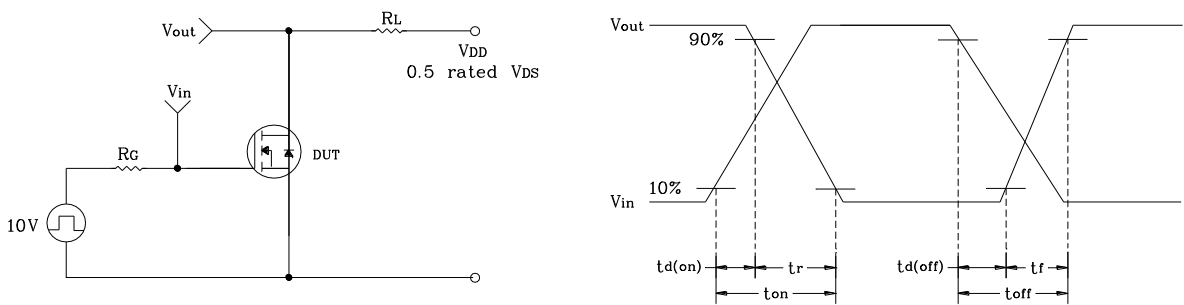
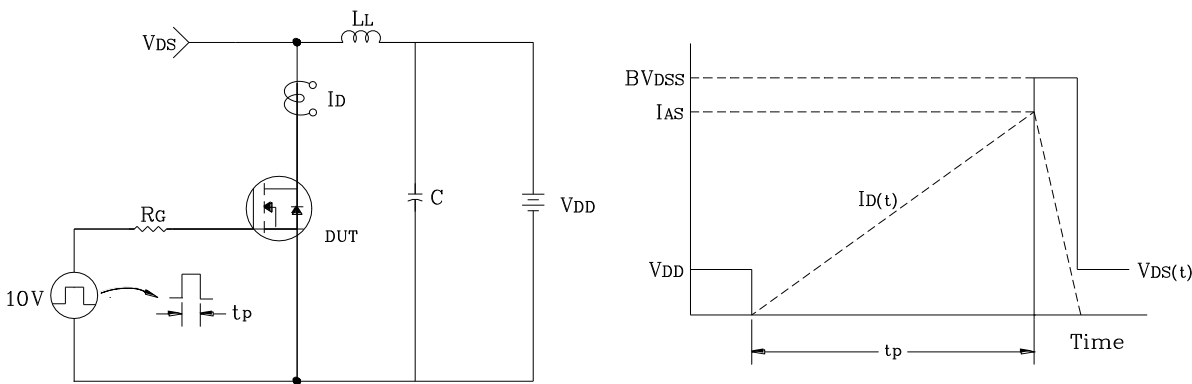
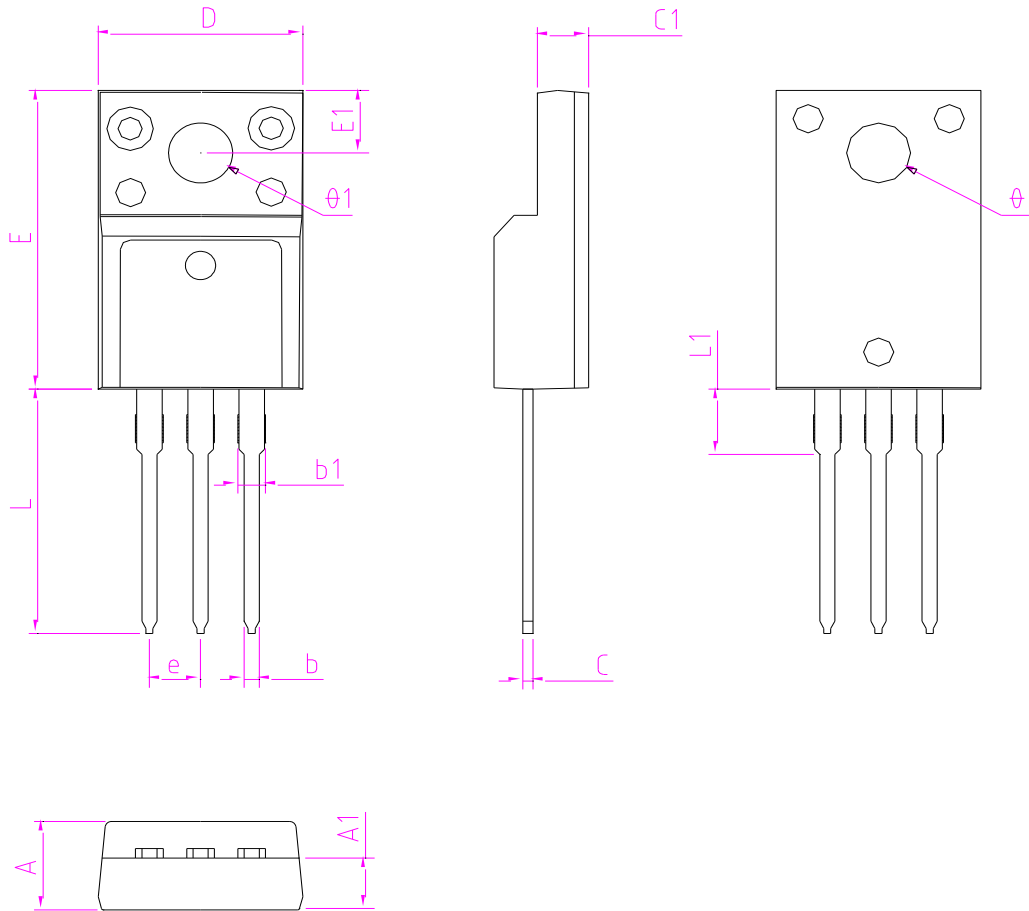


Fig. 14 E_{AS} Test Circuit & Waveform



Package Outline Dimensions



SYMBOL	MILLIMETERS			NOTE
	MINIMUM	NOMINAL	MAXIMUM	
A	4.65	4.70	4.75	
A1	2.71	2.76	2.81	
b	0.70	0.80	0.90	
b1	1.28	1.38	1.43	
C	0.40	0.50	0.60	
C1	2.04	2.54	3.04	
D	10.06	10.16	10.26	
e	2.54 REF			
E	15.77	15.87	15.97	
E1	3.05	3.30	3.55	
L	12.68	12.98	13.28	
L1	3.18 REF			
θ	3.30	3.40	3.50	
θ1	3.08	3.18	3.28	

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