中电国基南方集团有限公司

WM3A040075FA-V

N-Channel SiC Power MOSFET

G3 MOSFET Technology

V_{DS}	=	750	V
$R_{DS(on)}$	=	40	mΩ
I_D@25℃	=	55	A

Features

- High Blocking Voltage with Low On-Resistance
- High Speed Switching with Low Capacitance
- Easy to Parallel and Simple to Drive
- AEC-Q101 Qualified

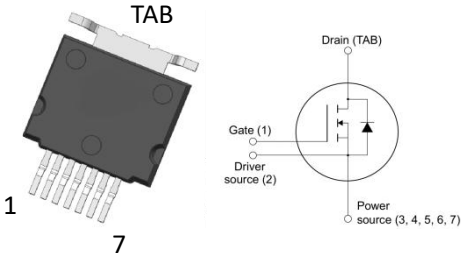
Benefits

- Higher System Efficiency
- Reduced Cooling Requirements
- Increased Power Density
- Increased System Switching Frequency

Applications

- Renewable Energy
- EV Battery Chargers
- High Voltage DC/DC Converters
- Switch Mode Power Supplies

Chip Outline



RoHS

Part Number	Package	Marking
WM3A040075FA-V	DT3PAK	WM3A040075FA-V

Maximum Ratings (T_C=25℃ unless otherwise specified)

Symbol	Parameter	Value	Unit	Test Conditions	Note
V_{DSmax}	Drain-Source Voltage	750	V	V_{GS}=0V, I_D=100μA	
V_{GSmax}	Gate-Source Voltage	-10/+23	V	Absolute maximum values	
V_{GSop}	Gate-Source Voltage	-5/+18	V	Recommended operational values	
I_D	Continuous Drain Current	55	A	V_{GS}=18V, T_c=25℃	Fig.19
		42		V_{GS}=18V, T_c=100℃	
$I_{D(pulse)}$	Pulsed Drain Current	166	A	Pulse width t_p limited by T_{Jmax}	Fig.22
P_D	Power Dissipation	166	W	T_c=25℃, T_J=175℃	Fig.20
T_J, T_{STG}	Operating Junction and Storage Temperature	-55 to +175	℃		
T_L	Solder Temperature, 1.6mm from case for 10s	260	℃		

Electrical Characteristics (T_C=25℃ unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	750	/	/	V	V_{GS}=0V, I_D=1mA	
$V_{GS(th)}$	Gate Threshold Voltage	2.0	2.9	4.0	V	V_{DS}=V_{GS}, I_D=7.5mA	Fig. 11
		/	2.1	/		V_{DS}=V_{GS}, I_D=7.5mA, T_J=175℃	
I_{DSS}	Zero Gate Voltage Drain Current	/	1	100	μA	V_{DS}=750V, V_{GS}=0V	
I_{GSS+}	Gate-Source Leakage Current	/	10	100	nA	V_{DS}=0V, V_{GS}=23V	
I_{GSS-}	Gate-Source Leakage Current	/	10	100	nA	V_{DS}=0V, V_{GS}=-10V	
$R_{DS(on)}$	Drain-Source On-State Resistance	/	40	52	mΩ	V_{GS}=18V, I_D=17.6A	Fig. 4,5,6
		/	48	/	mΩ	V_{GS}=18V, I_D=17.6A, T_J=175℃	
g_{fs}	Transconductance	/	22	/	S	V_{DS}=20V, I_{DS}=17.6A	Fig. 7
		/	20	/		V_{DS}=20V, I_{DS}=17.6A, T_J=175℃	
C_{iss}	Input Capacitance	/	1250	/	pF	V_{GS}=0V V_{DS}=500V f=1MHz	Fig. 17,18
C_{oss}	Output Capacitance	/	103	/			
C_{rss}	Reverse Transfer Capacitance	/	4.8	/			
E_{oss}	C_{oss} Stored Energy	/	13	/	μJ	V_{AC}=25mV	Fig. 16
E_{ON}	Turn-On Switching Energy	/	71	/	uJ	V_{DS}=500V, V_{GS}=-5V/18V	
E_{OFF}	Turn-Off Switching Energy	/	69	/		I_D=17.6A, $R_{G(ext)}$=2.5Ω, L=100μH	
$t_{d(on)}$	Turn-On Delay Time	/	6	/	ns	V_{DS}=500V, V_{GS}=-5V/18V, I_D=17.6A $R_{G(ext)}$=2.5Ω, R_L=25Ω	
t_r	Rise Time	/	8	/			
$t_{d(off)}$	Turn-Off Delay Time	/	15	/			
t_f	Fall Time	/	5	/			
$R_{G(int)}$	Internal Gate Resistance	/	2.0	/	Ω	f=1MHz, V_{AC}=25mV	
Q_{GS}	Gate to Source Charge	/	14	/	nC	V_{DS}=500V V_{GS}=-5V/18V I_D=17.6A	Fig. 12
Q_{GD}	Gate to Drain Charge	/	12	/			
Q_G	Total Gate Charge	/	40	/			

Reverse Diode Characteristics

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
V_{SD}	Diode Forward Voltage	3.9	/	V	V_{GS}=-5V, I_{SD}=8.8A, T_J=25℃	Fig. 8,9,10
		3.6	/		V_{GS}=-5V, I_{SD}=8.8A, T_J=175℃	
I_S	Continuous Diode Forward Current	37	/	A	T_C=25℃	
t_{rr}	Reverse Recover Time	13	/	ns	V_R=500V, I_{SD}=8.8A	
Q_{rr}	Reverse Recovery Charge	98	/	nC		
I_{rrm}	Peak Reverse Recovery Current	5	/	A		

Thermal Characteristics

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
$R_{\theta JC}$	Thermal Resistance from Junction to Case	0.9	/	℃/W		Fig. 21
$R_{\theta JA}$	Thermal Resistance from Junction to Ambient	/	40			

Typical Performance

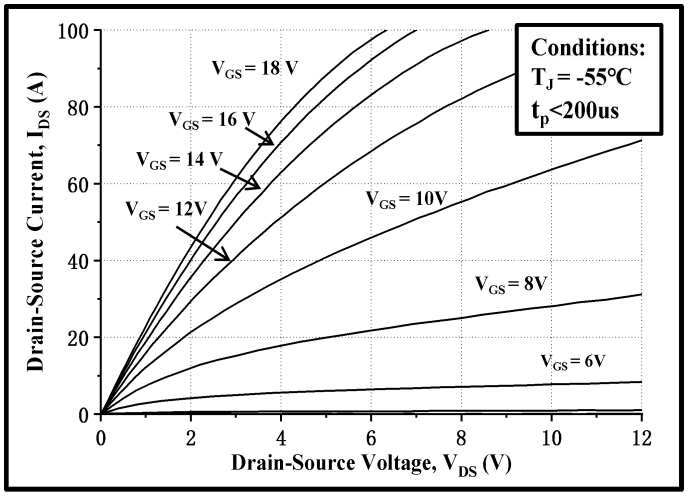


Figure 1. Output Characteristics T_J = -55℃

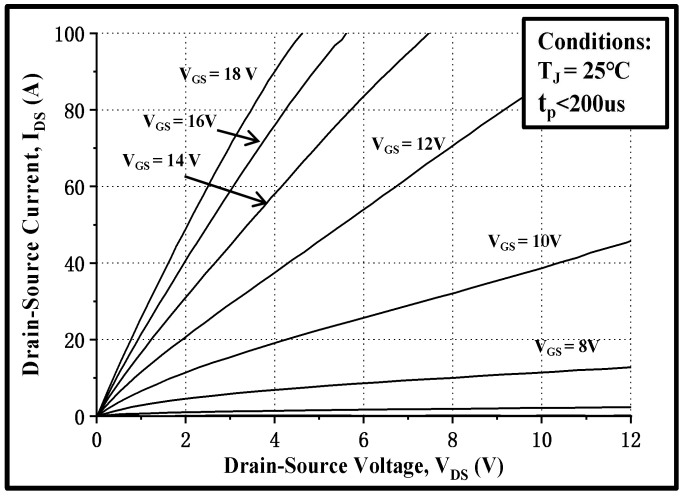


Figure 2. Output Characteristics T_J = 25℃

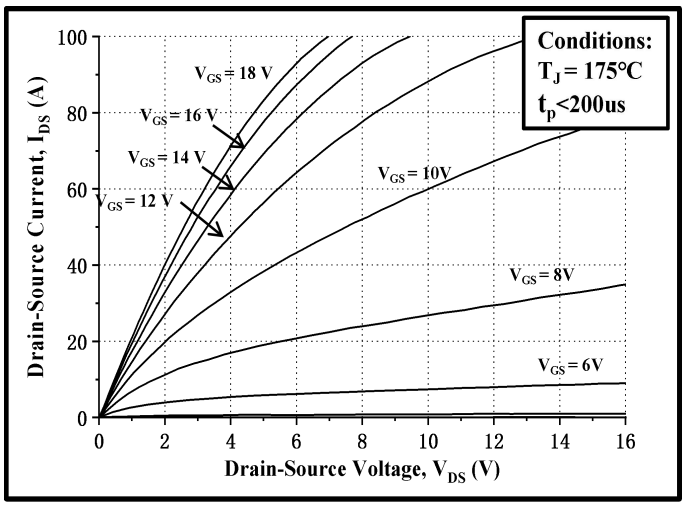


Figure 3. Output Characteristics T_J = 175℃

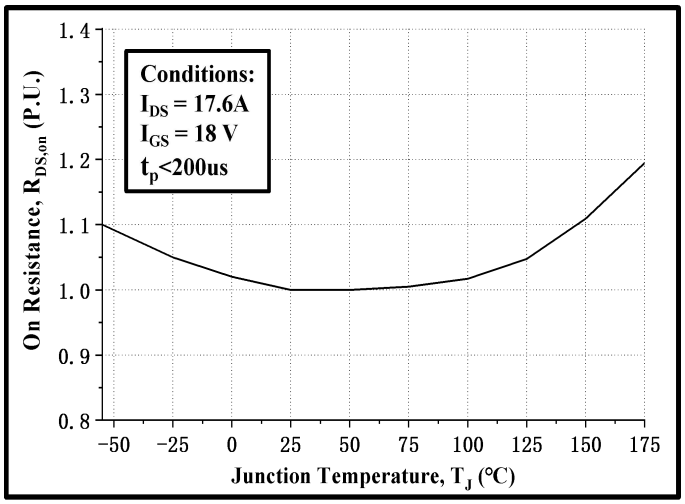


Figure 4. Normalized On-Resistance vs. Temperature

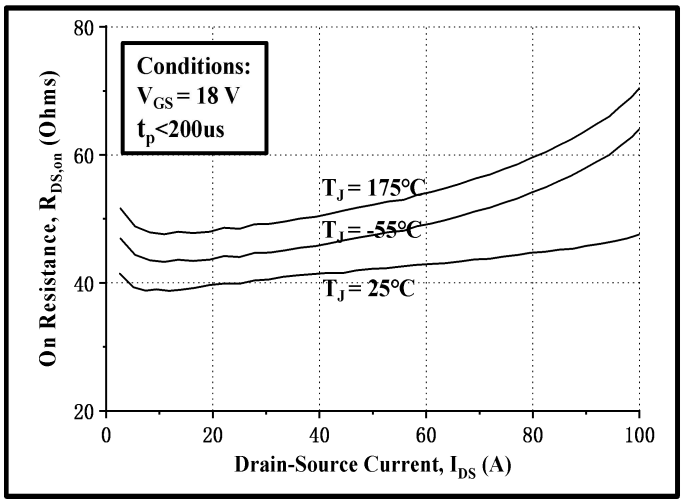


Figure 5. On-Resistance vs. Drain Current
For Various Temperatures

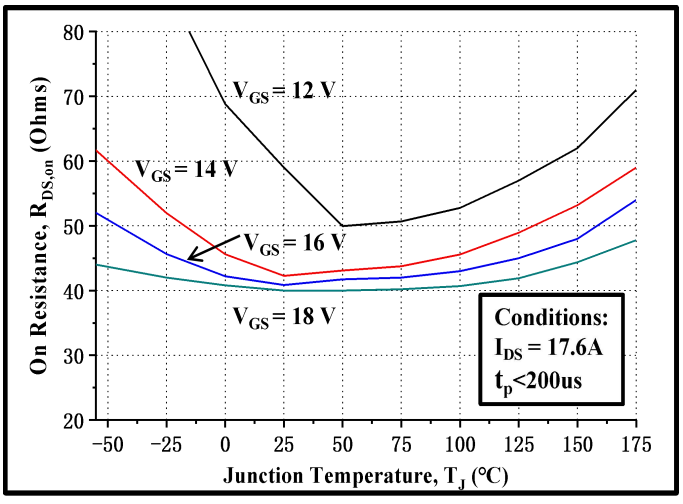


Figure 6. On-Resistance vs. Temperature
For Various Gate Voltage

Typical Performance

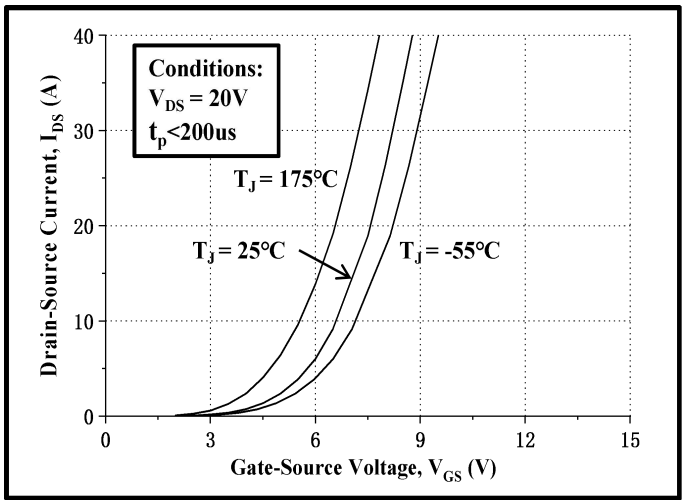


Figure 7. Transfer Characteristic for Various Junction Temperatures

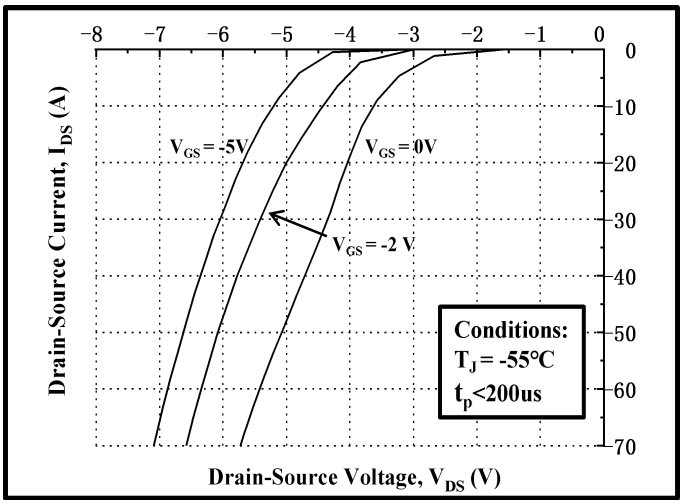


Figure 8. Body Diode Characteristic at -55℃

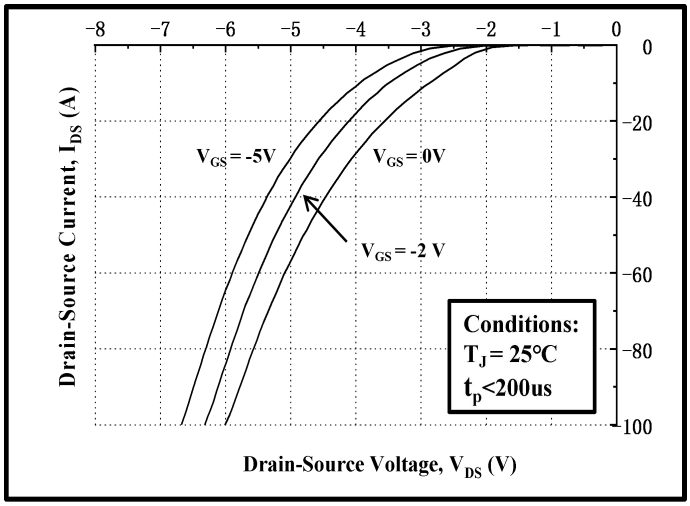


Figure 9. Body Diode Characteristic at 25℃

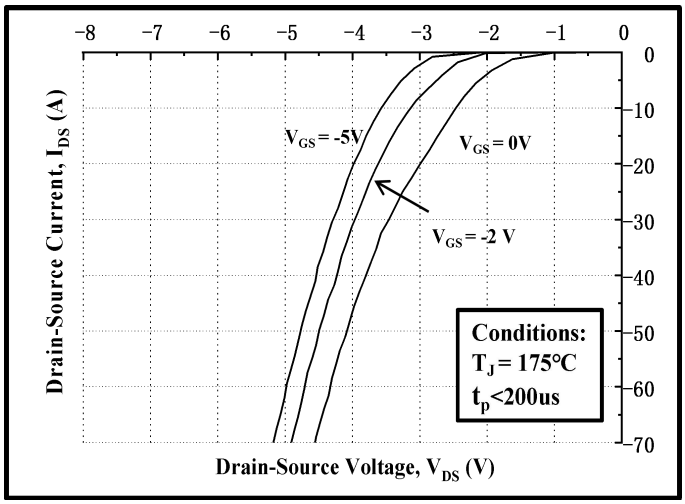


Figure 10. Body Diode Characteristic at 175℃

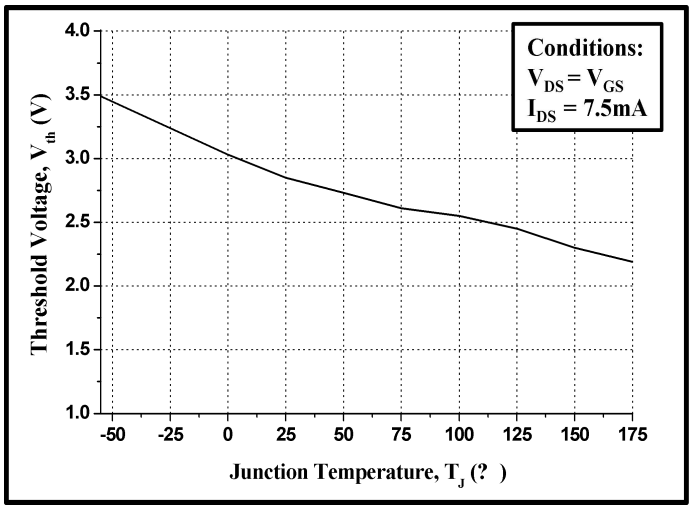


Figure 11. Threshold Voltage vs. Temperature

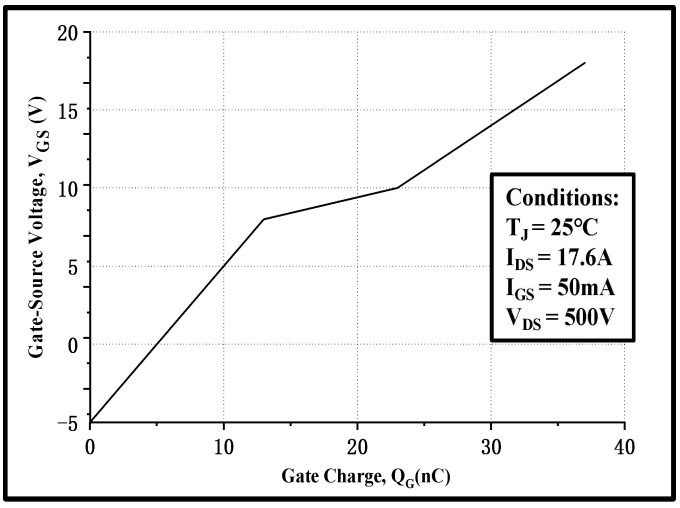


Figure 12. Gate Charge Characteristics

Typical Performance

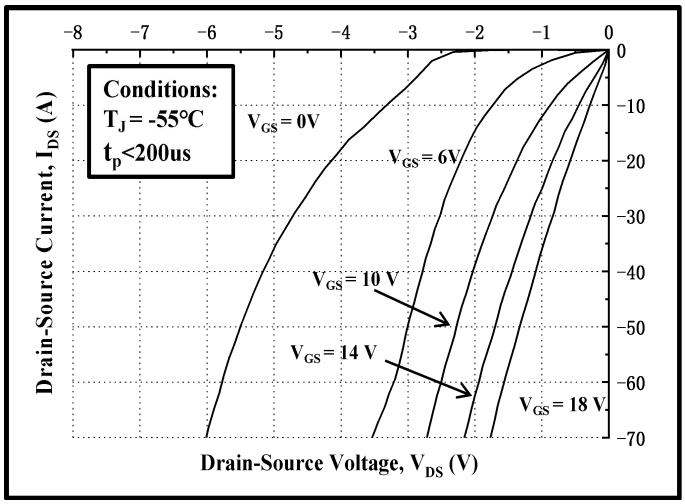


Figure 13. 3rd Quadrant Characteristic at -55℃

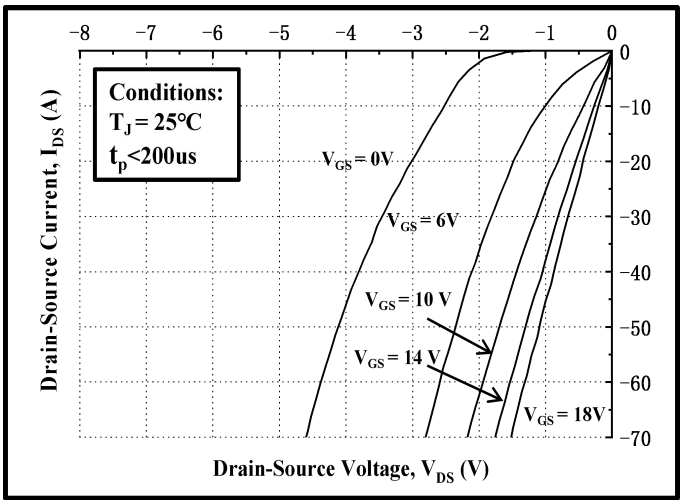


Figure 14. 3rd Quadrant Characteristic at 25℃

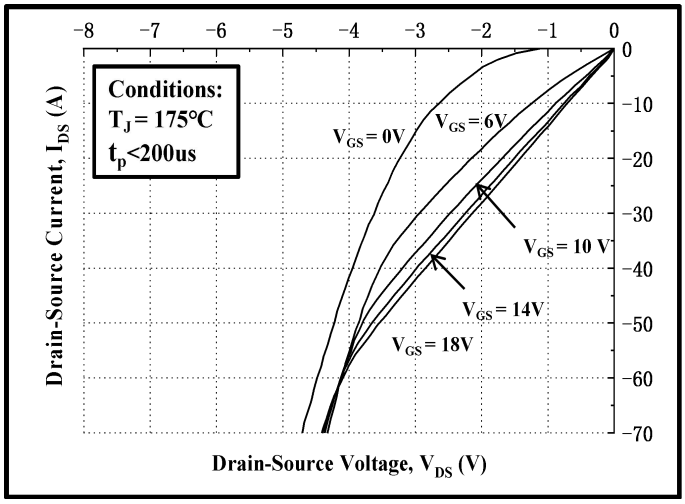


Figure 15. 3rd Quadrant Characteristic at 175 ℃

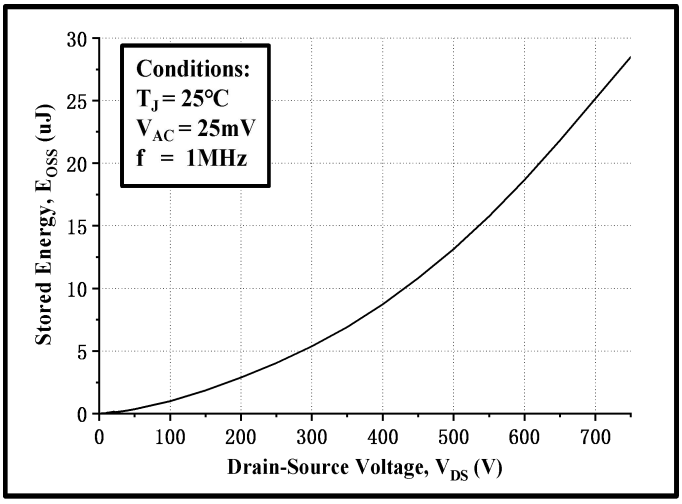


Figure16. Output Capacitor Stored Energy

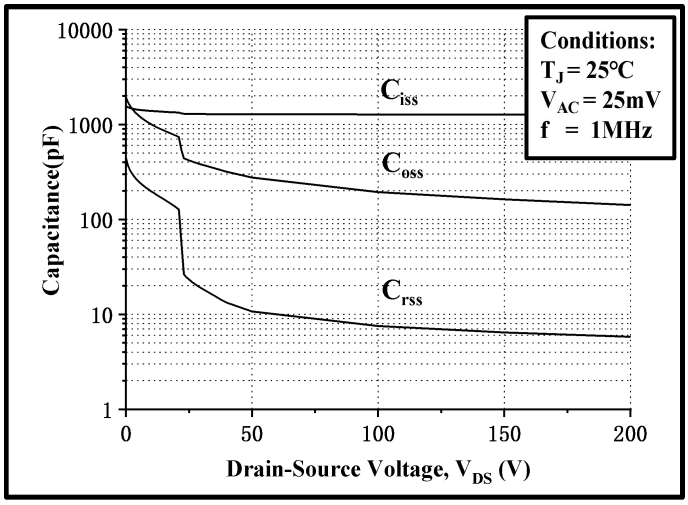


Figure 17. Capacitances vs. Drain-Source Voltage (0 - 200V)

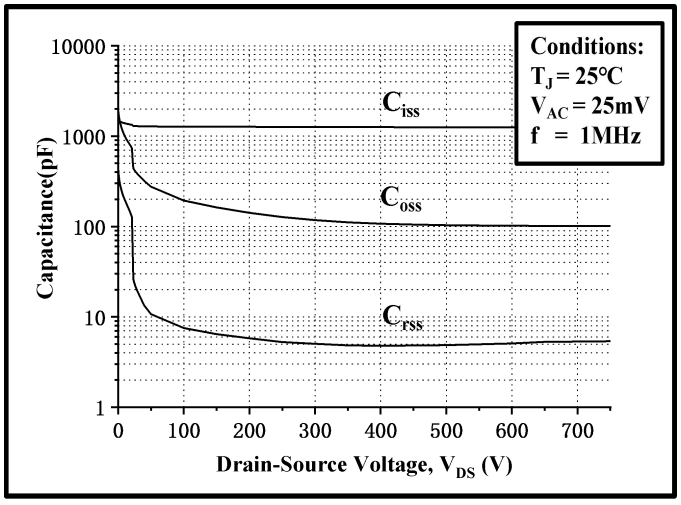


Figure 18. Capacitances vs. Drain-Source Voltage (0 - 750V)

Typical Performance

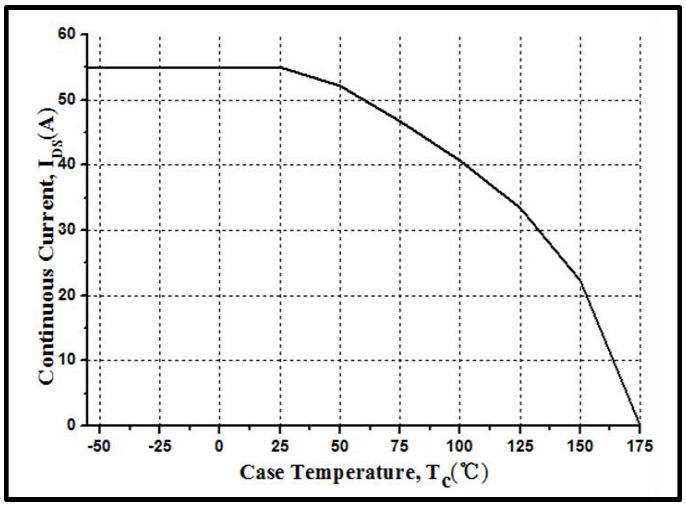


Figure 19. Continuous Drain Current Derating vs. Case Temperature

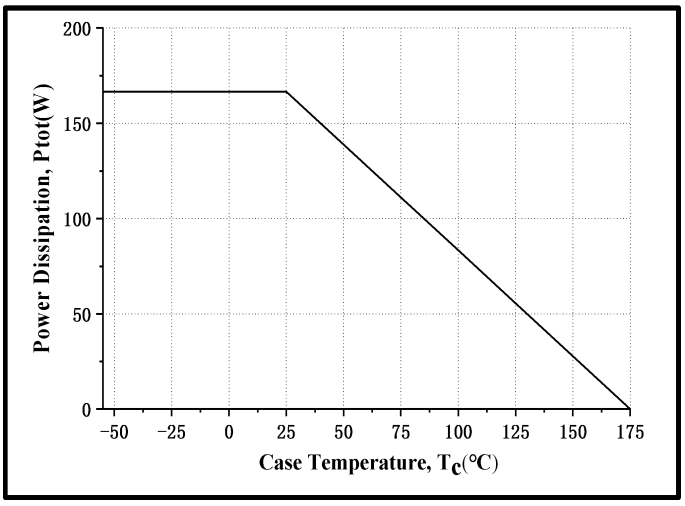


Figure 20. Maximum Power Dissipation Derating vs. Case Temperature

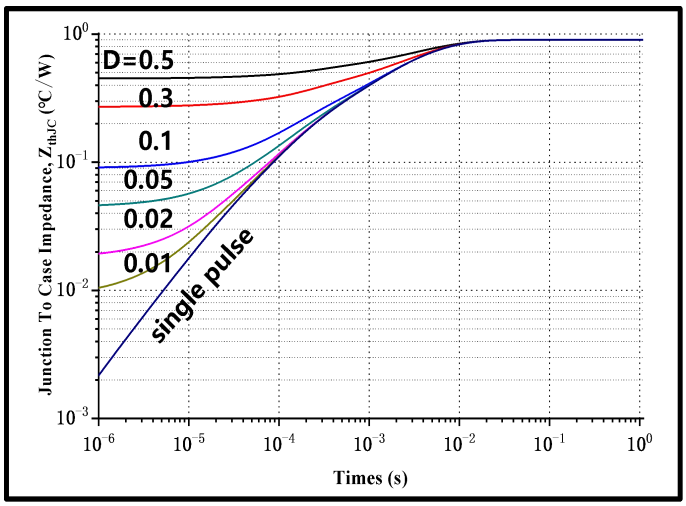


Figure 21. Transient Thermal Impedance (Junction - Case)

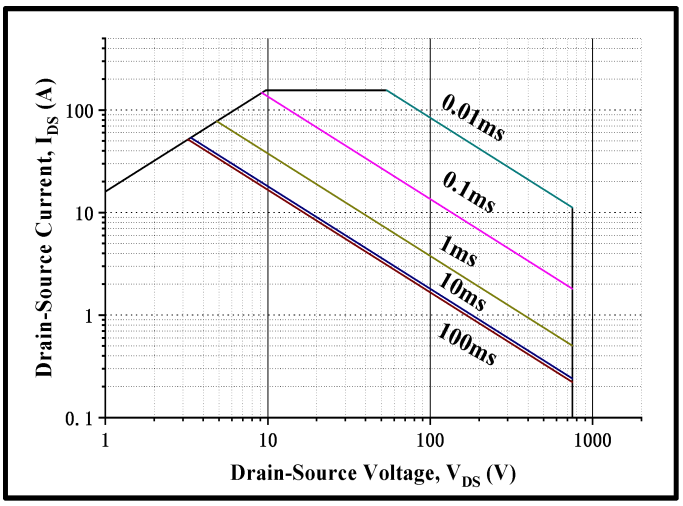


Figure22. Safe Operating Area

Test Circuit Schematic

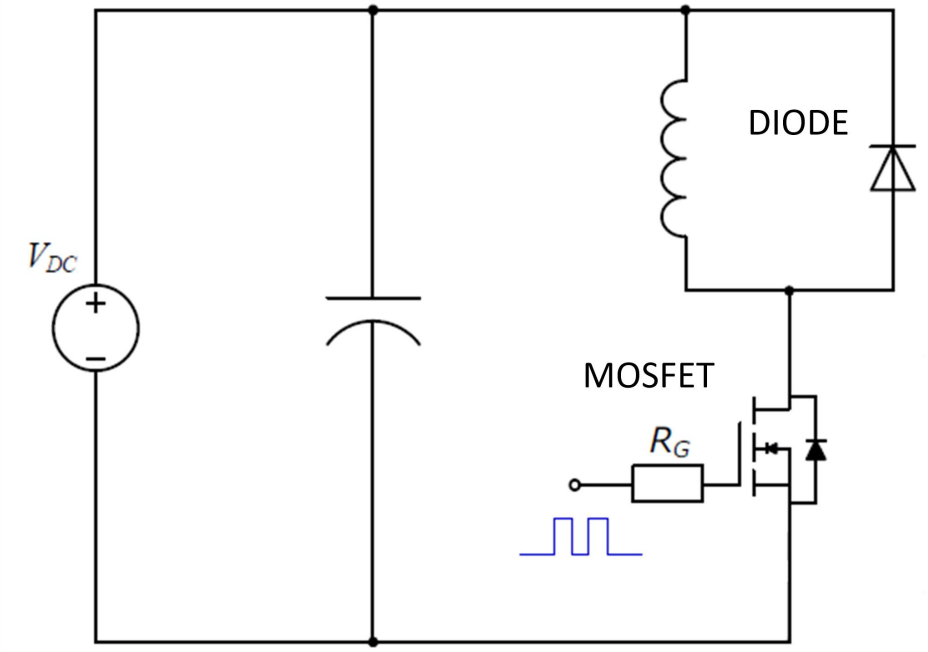
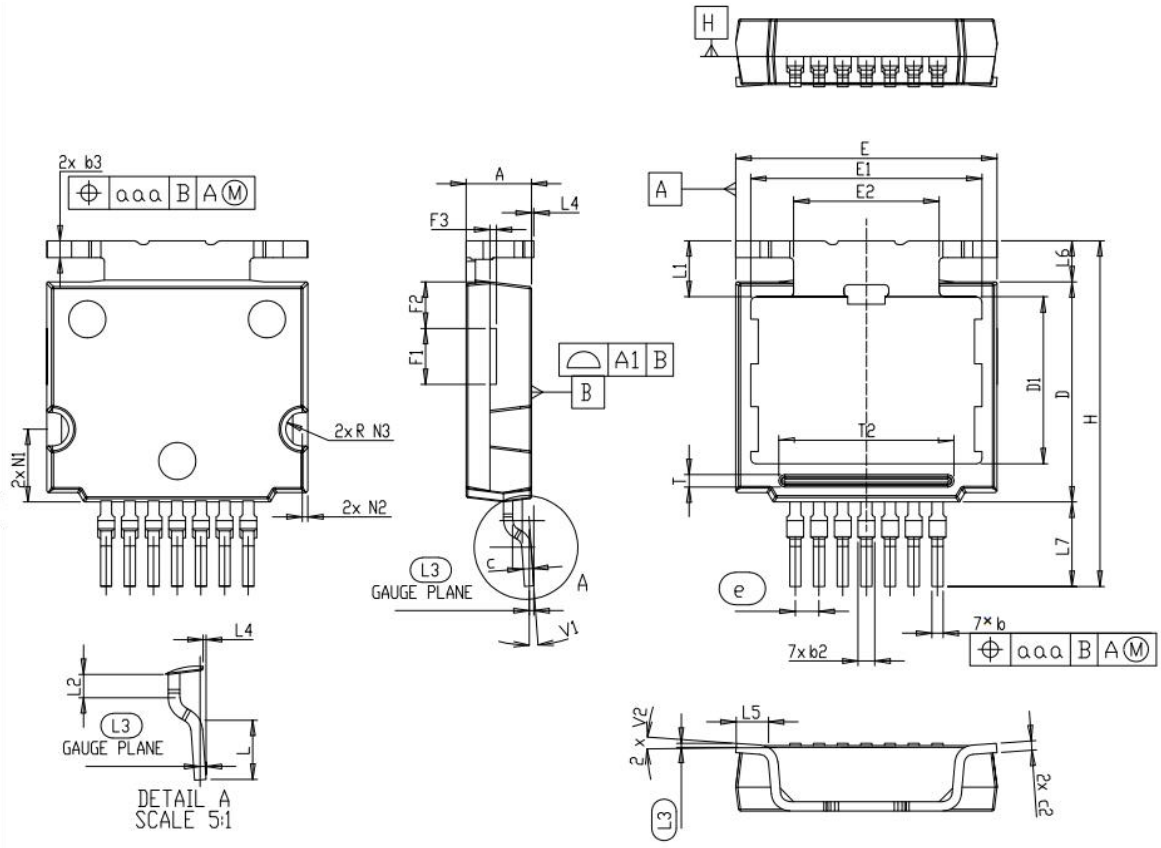


Figure 23. Clamped Inductive Switching Waveform Test Circuit

Package Dimensions



Ref.	Dimensions mm		
	Min.	Typ.	Max.
A	3.40	3.50	3.60
A1		0.05	
b	0.50	0.60	0.70
b2	0.50	0.70	1.00
b3	0.80	0.90	1.00
C	0.40	0.50	0.60
C2	0.40	0.50	0.60
D	11.70	11.80	11.90
D1	8.80	8.955	9.10
E	13.90	14.00	14.10
E1	12.30	12.40	12.50
E2	7.75	7.80	7.85
e		1.27	
H	18.00	18.58	19.00
aaa		0.10	
L	2.40	2.52	2.60
L1		3.05	
L2	0.90	1.00	1.10
L3		0.26	
L4	0.075	0.125	0.175
L5	1.83	1.93	2.03
L6	2.14	2.24	2.34
L7	4.44	4.54	4.64
F1	2.90	3.00	3.10
F2	2.40	2.50	2.60
F3	0.25	0.35	0.45
N1	3.80	3.90	4.00
N2	0.25	0.30	0.45
N3	0.80	0.90	1.00
T	0.50	0.67	0.70
T2	9.18	9.38	9.43
V1		0°	8°
V2		0°	8°

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