电力线通信模拟前端

查询样片: AFE032

特性

- 支持：
  - **CENELEC A，B，C，D** 频带
  - **ARIB STD-T84，FCC**
  - **FSK，SFSK** 和 **NB-OFDM**
- 符合：
  - **EN50065-1，-2，-3，-7**
  - 美国联邦通信委员会 **(FCC)**，第 **15** 部分
  - **ARIB STD-T84**
- 标准：
  - **G3，PRIME，P1901.2，ITU-G.hnem**
- 可编程 **Tx** 低通滤波器和 **Rx** 带通滤波器
- 具有热保护和过流保护的集成型电力线驱动器
- 低功耗：
  - **50mW**（接收器模式）
- 接收敏感度：**10μV$_{RMS}$**（典型值）
- 四线制 **SPI™** 接口
- **3** 个集成型零交叉检测器
- 封装方式：**48** 引脚四方扁平无引线 **(QFN) PowerPAD™**
- 扩展温度范围：**-40°C** 至 **+125°C**

应用范围

- 电子仪表
- 家庭局域网
- 照明
- 太阳能
- 电缆附线和电动汽车供电设备 **(EVSE)**

描述

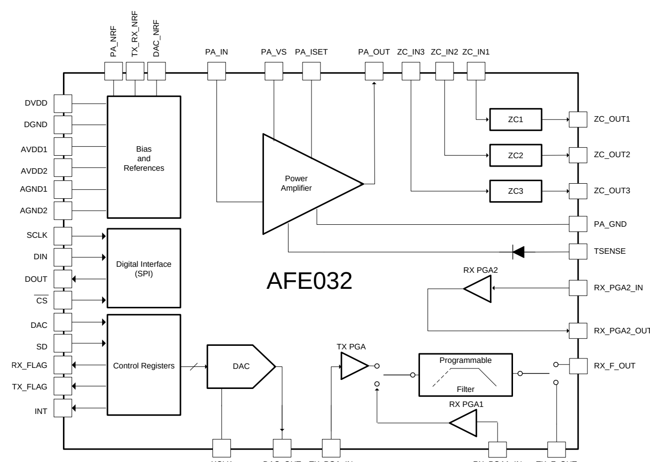
AFE032 是一款低成本，集成型，电力线通信 (PLC)，模拟前端 (AFE) 器件，此器件能够在一个数字信号处理器 (DSP) 或者微控制器控制下实现到电力线的变压器耦合连接。 这款器件非常适合于将高达 1.9A 的高电流、低阻抗线路驱动进入电抗性负载。

此集成型接收器能够检测到低至 10μV$_{RMS}$ 的信号（G3-FCC 模式），并且能够支持宽范围增益选项以适应不同的输入信号情况。 此单片集成电路在要求严格的电力线通信应用中提供高可靠性。

AFE032 传输功率放大器由电压范围在 7V 至 24V 的单电源供电。在负载电流为典型值时 (I_{OUT} = 1.5 A_{PEAK})，一个宽输出摆幅用一个额定 15V 的电源提供 12V$_{PP}$ 性能。

此器件在过热和短路情况下受到内部保护。 此器件还提供一个可选电流限值。 提供一个表示电流限制，过热限制和过压的中断输出。 还提供一个关断引脚，并且可被用来将此器件快速置于最低功耗状态。 为了通过串行外设接口 (SPI) 来优化功率耗散，可以启用或禁用每个功能块。

AFE032 采用耐热增强型，表面贴装，PowerPAD QFN-48 封装方式。 额定工作扩展工业结温范围为 -40°C 至 +125°C。



English Data Sheet: SBOS669

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION[1]

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS[1]

Over operating free-air temperature range, unless otherwise noted.

				VALUE	UNIT
PA_VS	Supply voltage (pins 44, 45)			+26	V
	Signal input terminals	Voltage[2]	Pins 3, 4, 6, 7, 8, 10	DGND – 0.4 to DVDD + 0.4	V
			Pins 13, 21, 28, 31, 32, 38, 39	AGND – 0.4 to AVDD + 0.4	V
			Pins 18, 19	PA_GND – 0.4 to PA_VS + 0.4	V
			Pin 27	AVDD + 0.4 to 26	V
		Current[2]	Pins 3, 4, 6, 7, 8, 10	±10	mA
			Pins 13, 21, 28, 31, 32, 38, 39	±10	mA
			Pins 18, 19	±10	mA
			Pin 35	±10	mA
	Signal output terminals	Voltage	Pins 5, 9, 47, 48	DGND – 0.4 to DVDD + 0.4	V
			Pins 14, 17, 20, 22, 33, 36, 37	AGND – 0.4 to AVDD + 0.4	V
			Pins 42, 43	PA_GND – 0.4 to PA_VS + 0.4	V
		Current; short-circuit to GND	Pins 5, 9, 47, 48	Continuous	
		Current; short-circuit to GND	Pins 14, 17, 20, 22, 33, 36, 37	Continuous	
		Current; short-circuit to GND	Pins 42, 43	Continuous	
AVDD	Analog supply voltage (pins 11, 30)			5.5	V
DVDD	Digital supply voltage			5.5	V
T_A	Operating temperature[3]			–40 to +150	°C
T_{stg}	Storage temperature			–55 to +150	°C
T_J	Junction temperature			+150	°C
ESD	Electrostatic discharge ratings	Human body model (HBM)		3000	V
		Machine model (MM)		200	V
		Charged device model (CDM)		500	V

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and do not imply functional operation of the device at these or any other conditions beyond those indicated. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.4 V beyond the supply rails should be current limited to 10 mA or less.
(3) The device automatically goes to shutdown above +165°C.

THERMAL INFORMATION

THERMAL METRIC[1]		AFE032 RGZ (QFN) 48 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	22.5	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	12.1	
θ_{JB}	Junction-to-board thermal resistance	7.5	
ψ_{JT}	Junction-to-top characterization parameter	2.0	
ψ_{JB}	Junction-to-board characterization parameter	5.4	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	1.7	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

ELECTRICAL CHARACTERISTICS: Transmitter

At T_{CASE} = +25°C, V_{PAVS} = 15 V, and V_{AVDD} = V_{DVDD} = 3.3 V, unless otherwise noted.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
DAC							
	Resolution		12-bit DAC, internal V_{REF} = 0.7 V	165	171	176	µV
DR	Data rate[1]		DAC pin high, 12-bit word		4.8	5.2	MSPS
G_E	Gain error		Full-scale range, T_J = –40°C to +125°C	–2%	±0.5%	2%	
DAC OUTPUT							
R_O	Output resistance		G = 1, f = 100 kHz		1		kΩ
TX_PGA INPUT							
	Input voltage range			(AGND + 0.15) / gain		(AVDD – 0.15) / gain	V
R_I	Input resistance		G = 1.15 V/V		52		kΩ
			G = 2.3 V/V		34		kΩ
			G = 3.25 V/V		26		kΩ
			G = 4.6 V/V		20		kΩ
G	Gain				1.15, 2.3, 3.25, 4.6[2]		V/V
G_E	Gain error		Includes DAC, programmable filter, and TX_PGA for all gains, T_J = –40°C to +125°C	–2%	±0.1%	2%	
	Gain error drift		Includes DAC, programmable filter, and TX_PGA for all gains, T_J = –40°C to +125°C	–10	±3	+10	ppm/°C
TX_PGA FREQUENCY RESPONSE							
BW	Bandwidth[3]		C_L = 20 pF, G = 1.15 V/V, T_J = –40°C to +125°C		30		MHz
			C_L = 20 pF, G = 2.3 V/V, T_J = –40°C to +125°C		21.5		MHz
			C_L = 20 pF, G = 3.25 V/V, T_J = –40°C to +125°C		17.5		MHz
			C_L = 20 pF, G = 4.6 V/V, T_J = –40°C to +125°C		15.5		MHz
TX PATH TRANSMITTER NOISE[4]							
	Integrated noise at PA output[5]	CEN-A	35 kHz to 95 kHz		370		$µV_{RMS}$
		CEN-B	95 kHz to 125 kHz		220		$µV_{RMS}$
		CEN-C	125 kHz to 140 kHz		160		$µV_{RMS}$
		CEN-D	140 kHz to 148 kHz		98		$µV_{RMS}$
		ARIB STD-T84	35 kHz to 420 kHz		640		$µV_{RMS}$
		FCC-LOW	35 kHz to 125 kHz		384		$µV_{RMS}$
		G3-FCC	150 kHz to 490 kHz		565		$µV_{RMS}$
POWER AMPLIFIER (PA) INPUT							
	Input voltage range		For linear operation	(PA_GND + 0.4) / gain		(PA_VS – 0.4) / gain	V
	Input impedance				17		kΩ
PA FREQUENCY RESPONSE							
BW	Bandwidth		I_{LOAD} = 0 mA	3.4	3.82	4.23	MHz
SR	Slew rate		PA_VS = 24 V, 20-V step		75		V/µs
	Full-power bandwidth		PA_VS = 24 V, V_{OUT} = 20 V_{PP}		1		MHz
PSRR	Power-supply rejection ratio		RTI, dc to f = 50 kHz	80	94		dB

(1) Refer to the *Application Information* section.
(2) This parameter is from DAC_OUT to TX_F_OUT. This parameter includes the LPF gain error and is the dc gain. Adding LPF causes some loss of gain flatness.
(3) This parameter is internal to the device. Bandwidth is designed and simulated over corners to ensure a low-distortion PGA in the application.
(4) Includes the DAC, programmable filter, TX_PGA, and PA noise-reducing capacitor = 1 nF from DAC_NRF to ground, PA_NRF to ground, and TX_RF_NRF to ground.
(5) Includes the DAC, TX_PGA (gain = 4.6), LPF, and PA.

ELECTRICAL CHARACTERISTICS: Transmitter (continued)

At T_{CASE} = +25°C, V_{PAVS} = 15 V, and V_{AVDD} = V_{DVDD} = 3.3 V, unless otherwise noted.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
PA OUTPUT							
V_O	Voltage output swing	From PA_VS	I_O = 200-mA sourcing, 1-ms pulse			0.5	V
			I_O = 1.5-A sourcing, 1-ms pulse			2.25	V
		From PA_GND	I_O = 200 mA sinking, 1-ms pulse			0.5	V
			I_O = 1.5-A sinking, 1-ms pulse			1.5	V
	Maximum continuous current, dc		Pin 26 connected to ground, REG_PA_CURRENT_CFG[5:4] = 11		1.9		A
	Output resistance		I_O = 1.9 A, f = 500 kHz		0.1		Ω
	PA disabled output impedance		f = 100 kHz, PA_NRF enabled		130 || 105		kΩ || pF
	Output current limit	Resistor-selectable	R_{SET} connected from pin 26 to ground	See the *Application Information* section			
		Digitally-selectable[6]	Pin 26 connected to ground, REG_PA_CURRENT_CFG[5:4] = 00		1.25		A
			Pin 26 connected to ground, REG_PA_CURRENT_CFG[5:4] = 01		1.8		A
			Pin 26 connected to ground, REG_PA_CURRENT_CFG[5:4] = 10		2.5		A
			Pin 26 connected to ground, REG_PA_CURRENT_CFG[5:4] = 11		3.0		A
PA THERMAL SHUTDOWN							
	Junction temperature at shutdown				+165		°C
	Hysteresis				+15		°C
	Return to normal operation				+150		°C
PA TSENSE DIODE							
η	Diode ideality factor				1.03		
PA GAIN							
G	Nominal gain		PA_OUT / PA_IN		7.4[7]		V/V
G_E	Gain error		T_J = –40°C to +125°C	–2%	0.1%	2%	
	Gain error drift		T_J = –40°C to +125°C		±5		ppm/°C

(6) Refer to the *Application Information* section.
(7) This gain reflects a direct measurement on the PA block by itself. The gain in the signal chain composed by Tx PGA, Tx Filter and PA equals the Tx PGA gain multiplied by 7 V/V (where 7 V/V is the gain of the PA block when its input is capacitively coupled to the Tx Filter output). Refer to the Power Amplifier Block section for more information.

ELECTRICAL CHARACTERISTICS: Programmable Filter

At T_{CASE} = +25°C, V_{PAVS} = 15 V, and V_{AVDD} = V_{DVDD} = 3.3 V, unless otherwise noted.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
LOW-PASS FILTER (LPF)							
Cutoff frequencies in Tx mode(1)	CEN-A		1-dB gain flatness, T_J = –40°C to +125°C	94	102	110	kHz
	CEN-B, CEN-C, CEN-D, FCC-LOW		1-dB gain flatness, T_J = –40°C to +125°C	148	160	172	kHz
	ARIB STD-T84		1-dB gain flatness, T_J = –40°C to +125°C	405	435	475	kHz
	G3-FCC		1-dB gain flatness, T_J = –40°C to +125°C	470	505	540	kHz
	Transition time	Rx to Tx	PA_NRF, TX_RX_NRF, and DAC, T_J = –40°C to +125°C		80(2)		µs
		Tx to Rx	NRF enabled, T_J = –40°C to +125°C		30		µs
LPF OUTPUT							
R_O	Output impedance		f = 100 kHz		1		kΩ
HIGH-PASS FILTER (HPF)							
	CEN-A, CEN-B, CEN-C, CEN-D, ARIB STD-T84, FCC-LOW		1-dB gain flatness, T_J = –40°C to +125°C	30	35	40	kHz
	G3-FCC		1-dB gain flatness, T_J = –40°C to +125°C	120	132	152	kHz
	Transition time	Rx to Tx	PA_NRF, TX_RX_NRF, and DAC, T_J = –40°C to +125°C		30		µs
		Tx to Rx	NRF enabled, T_J = –40°C to +125°C		80(2)		µs
HPF OUTPUT							
R_O	Output impedance		f = 100 kHz		1		kΩ

(1) These cutoff frequencies are only valid when the filter is used as a low-pass filter. Refer to the *Register Map* section in the *Application Information* for register settings.
(2) See the *Application Information* section for the start-up procedure.

ELECTRICAL CHARACTERISTICS: Receiver

At T_{CASE} = +25°C, V_{PAVS} = 15 V, and V_{AVDD} = V_{DVDD} = 3.3 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RX_PGA1 INPUT						
	Input voltage range	For linear operation	(AGND + 0.15) / gain		(AVDD – 0.15) / gain	V
R_I	Input resistance	G = 0.125 V/V		111.1		kΩ
		G = 0.25 V/V		100		kΩ
		G = 0.5 V/V		133		kΩ
		G = 1 V/V		100		kΩ
		G = 2 V/V		66		kΩ
		G = 4 V/V		40		kΩ
		G = 8 V/V		22		kΩ
		G = 16 V/V		12		kΩ
		G = 32 V/V		6		kΩ
RX_PGA1 GAIN						
	DC gain			0.125, 0.25, 0.5, 1, 2, 4, 8, 16, 32		V/V
G_E	Gain error	For all gains, T_J = –40°C to +125°C	–5%		5%	
	Gain error drift	T_J = –40°C to +125°C		±100		ppm/°C
RX_PGA1 FREQUENCY RESPONSE						
BW	Bandwidth	C_L = 20 pF, G = 0.125 V/V		47		MHz
		C_L = 20 pF, G = 0.25 V/V		18		MHz
		C_L = 20 pF, G = 0.5 V/V		6		MHz
		C_L = 20 pF, G = 1 V/V		4		MHz
		C_L = 20 pF, G = 2 V/V		3		MHz
		C_L = 20 pF, G = 4 V/V		2.5		MHz
		C_L = 20 pF, G = 8 V/V		2.1		MHz
		C_L = 20pF, G = 16 V/V		1.85		MHz
		C_L = 20 pF, G = 32 V/V		1.55		MHz
RX_PGA2 INPUT						
	Input voltage range	For linear operation	(A_{GND} + 0.15) / gain		(AVDD – 0.15)/ gain	V
R_I	Input resistance	G = 1 V/V		54		kΩ
		G = 4 V/V		21		kΩ
		G = 16 V/V		5.5		kΩ

ELECTRICAL CHARACTERISTICS: Receiver (continued)

At T_{CASE} = +25°C, V_{PAVS} = 15 V, and V_{AVDD} = V_{DVDD} = 3.3 V, unless otherwise noted.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
Rx_PGA2 GAIN							
G	Gain				1, 4, 16		V/V
G_E	Gain error		For all gains, T_J = –40°C to +125°C	–2%		2%	
	Gain error drift		T_J = –40°C to +125°C		±100		ppm/°C
RX_PGA2 FREQUENCY RESPONSE							
BW	Bandwidth		C_L = 20 pF, G = 1 V/V		6.73		MHz
			C_L = 20 pF, G = 4 V/V		5		MHz
			C_L = 20 pF, G = 16 V/V		3		MHz
RX_PGA2 OUTPUT							
	Output resistance		G = 1, f = 100 kHz		1		kΩ
RX PATH SENSITIVITY(1)							
	Input-referred integrated noise	CEN-A	35 kHz to 95 kHz		10		μV_{RMS}
		CEN-B	95 kHz to 125 kHz		5		μV_{RMS}
		CEN-C	125 kHz to 140 kHz		3		μV_{RMS}
		CEN-D	140 kHz to 148 kHz		2		μV_{RMS}
		ARIB STD-T84	35kHz to 400 kHz		12		μV_{RMS}
		FCC-LOW	35 kHz to 125 kHz		11		μV_{RMS}
		G3-FCC	150 kHz to 490 kHz		10		μV_{RMS}

(1) Noise-reducing capacitor = 1 nF from TX_RX_NRF to ground, RX_PGA1 = 32, and RX_PGA2 = 1.

ELECTRICAL CHARACTERISTICS: Noise-Reducing Filters

At T_{CASE} = +25°C, V_{PAVS} = 15 V, and V_{AVDD} = V_{DVDD} = 3.3 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PA_NRF						
	Bias voltage			$V_{PAV\ S}$ / 2		V
R_{OUT}	Output resistance			4		kΩ
t_{ON}	Turn-on time	Noise-reducing capacitor = 1 nF from PA_NRF to ground		250		ms
t_{OFF}	Turn-off time			10		µs
TX_RX_NRF						
	Bias voltage			V_{AVDD} / 2		V
R_{OUT}	Output resistance			1		kΩ
t_{ON}	Turn-on time	Noise-reducing capacitor = 1 nF from TX_RX_NRF to ground		10		µs
t_{OFF}	Turn-off time			10		µs
DAC_NRF						
	Bias voltage			V_{AVDD} / 4.7		V
R_{OUT}	Output resistance			1		kΩ
t_{ON}	Turn-on time	Noise-reducing capacitor = 1 nF from DAC_NRF to ground		10		µs
t_{OFF}	Turn-off time			10		µs

ELECTRICAL CHARACTERISTICS: Digital

At T_{CASE} = +25°C, V_{PAVS} = 15 V, and V_{AVDD} = V_{DVDD} = 3.3 V, unless otherwise noted.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUTS (SCLK, DI, $\overline{CS}$, SD, DAC, XCLK)							
	Leakage input current		0 V ≤ V_{IN} ≤ DVDD	–1	0.01	1	µA
V_{IH}	High-level input voltage			0.7 × DVDD			V
V_{IL}	Low-level input voltage					0.3 × DVDD	V
	SD pin function (active high)	SD pin high	SD > 0.7 × DVDD	Device in shutdown			
		SD pin low	SD < 0.3 × DVDD	Device in normal operation			
	DAC pin function (active high)	DAC pin high	DAC > 0.7 × DVDD	SPI access to DAC registers			
		DAC pin low	DAC < 0.3 × DVDD	SPI access to command and data registers			
	XCLK frequency range		XCLK jitter < 180 ps	5		40	MHz
DIGITAL OUTPUTS (DO, ZC_OUT)							
V_{OH}	High-level output voltage		I_{OH} = 3 mA	DVDD – 0.4		DVDD	V
V_{OL}	Low-level output voltage		I_{OL} = –3 mA	GND		GND + 0.4	V
DIGITAL OUTPUTS (INT, TX_FLAG, RX_FLAG)							
I_{OH}	High-level output current		V_{OH} = 3.3 V			1	µA
V_{OL}	Low-level output voltage		I_{OL} = 4 mA			0.4	V
I_{OL}	Low-level output current		V_{OL} = 400 mV	4			mA
	INT pin (active low, open-drain)	INT pin high	INT sink high < 1 µA	Normal operation			
		INT pin low	INT < 0.4 V	Interrupt has occurred			
	TX_FLAG (active low, open-drain)	TX_FLAG pin high	TX_FLAG sink high < 1 µA	Tx block disabled			
		TX_FLAG pin low	TX_FLAG < 0.4 V	Tx block ready			
	RX_FLAG (active low, open-drain)	RX_FLAG pin high	RX_FLAG sink high < 1 µA	Rx block disabled			
		RX_FLAG pin low	RX_FLAG < 0.4 V	Rx block ready			
GAIN TIMING							
	Gain select time				0.2		µs
SHUTDOWN MODE TIMING							
	Enable time		SD pin transitions from high to low		3		ms
	Disable time		SD pin transitions from low to high		2		ms
POR TIMING							
	Power-on reset power-up time		DVDD ≥ 2 V		3		ms

ELECTRICAL CHARACTERISTICS: Zero-Crossing Detector

At T_{CASE} = +25°C, V_{PAVS} = 15 V, and V_{AVDD} = V_{DVDD} = 3.3 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Input voltage range		AGND		AVDD	V
	Input current range		–10		10	mA
R_{IN}	Input resistance	AGND ≤ V_{IN} ≤ AVDD		2		MΩ
C_{IN}	Input capacitance			4		pF
	Rising threshold		0.45	0.9	1.35	V
	Falling threshold		0.25	0.5	0.75	V
	Hysteresis		0.2	0.4	0.6	V
	Jitter	50 Hz and 60 Hz, 240 V_{RMS} and 120 V_{RMS}		10		ns

ELECTRICAL CHARACTERISTICS: Power Supply

At T_{CASE} = +25°C, T_J = –40°C to +125°C, V_{PAVS} = 15 V, and V_{AVDD} = V_{DVDD} = 3.3 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OPERATING SUPPLY RANGE						
PA_VS	Power amplifier		7	15	24	V
DVDD	Digital supply			3.3		V
AVDD	Analog supply			3.3		V
QUIESCENT CURRENT (SD pin low)						
IQ_{PA_VS}	Power amplifier	I_O = 0 V, PA = on(1), REG_PA_CURRENT_CFG[7:6] = 00	40	48	56	mA
		I_O = 0 V, PA = on(1), REG_PA_CURRENT_CFG[7:6] = 01	68	78	88	mA
		I_O = 0 V, PA = on(1), REG_PA_CURRENT_CFG[7:6] = 10	84	96	108	mA
		I_O = 0 V, PA = on(1), REG_PA_CURRENT_CFG[7:6] = 11	10	17	24	mA
IQ_{DVDD}	Digital supply	Tx configuration(2)	1.5	2.5	3.5	mA
		Rx configuration(3)	1.1	2.1	3.1	mA
		All blocks disabled(4)		330	450	µA
IQ_{AVDD}	Analog supply	Tx configuration(3)	8	11	14	mA
		Rx configuration(4)	9	13	17	mA
		All blocks disabled(4)		25	100	µA
SHUTDOWN						
SD_{PA_VS}	Power amplifier	SD pin high		40	150	µA
SD_{DVDD}	Digital supply	SD pin high		330	400	µA
SD_{AVDD}	Analog supply	SD pin high		25	50	µA

(1) PA and PA output enabled.
(2) The DAC, TX_PGA, low-pass filter, PA, PA_NRF, TX_RX_NRF, and DAC_NRF blocks are enabled in the Tx configuration. All other blocks are disabled.
(3) The RX_PGA1, high-pass filter, low-pass filter, RX_PGA2, and TX_RX_NRF blocks are enabled in the Rx configuration. All other blocks are disabled.
(4) All internal blocks disabled, SD pin low.

SPI TIMING REQUIREMENTS

	PARAMETER	MIN	TYP	MAX	UNIT
	Input capacitance		1		pF
t_{RFI}	Input rising and falling time ($\overline{CS}$, DIN, SCLK)			2	ns
t_{RFO}	DOUT rising and falling time			10	ns
t_{CSH}	$\overline{CS}$ high time	10			DAC_CLK cycles(1)
t_{CS0}	SCLK edge to $\overline{CS}$ falling edge setup time	10			ns
t_{CSSC}	$\overline{CS}$ falling edge to first SCLK edge setup time	10			ns
f_{SCLK}	SCLK frequency		20	30	MHz
t_{HI}	SCLK high time	16.7	25		ns
t_{LO}	SCLK low time	16.7	25		ns
t_{SCCS}	SCLK last edge to $\overline{CS}$ rising edge setup time	10			ns
t_{CS1}	$\overline{CS}$ rising edge to SCLK edge setup time	10			ns
t_{SU}	DIN setup time	5			ns
t_{HD}	DIN hold time	5			ns
t_{DO}	SCLK to DOUT valid propagation delay			16	ns
t_{soz}	$\overline{CS}$ rising edge to DOUT forced to Hi-Z			20	ns

(1) $\overline{CS}$ pin must remain high for at least ten DAC_CLK cycles after a write operation and must remain high for at least five DAC_CLK cycles after a read operation.

TIMING DIAGRAMS

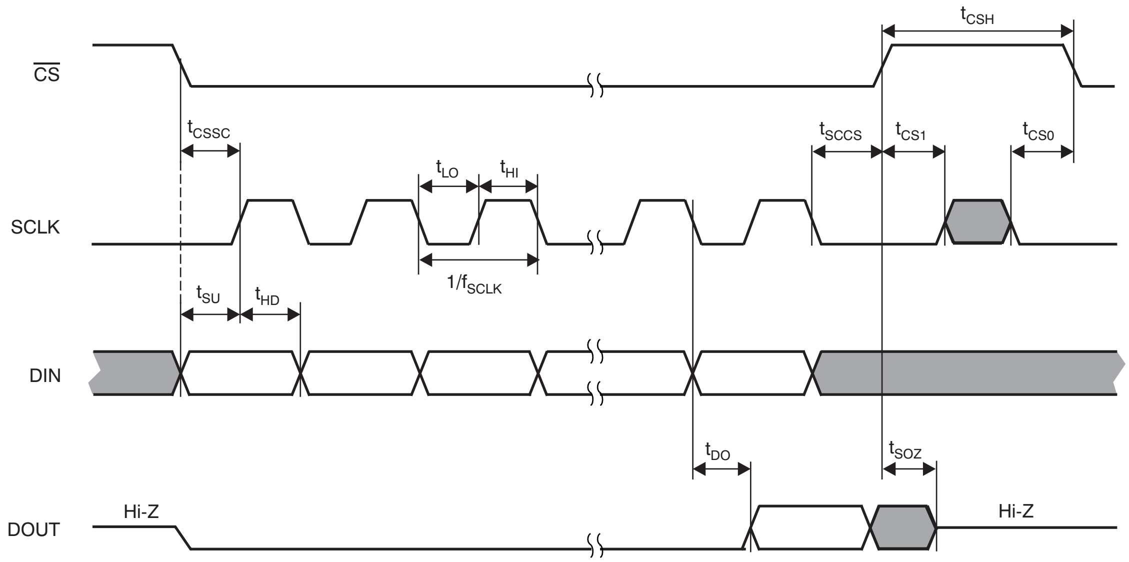


Figure 1. SPI Mode 0,0

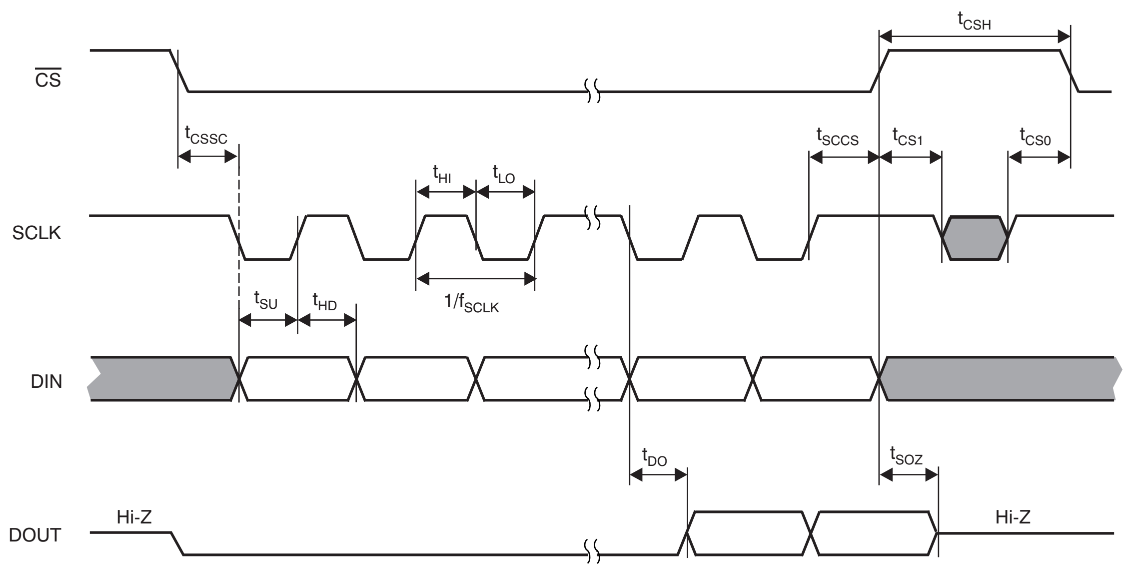
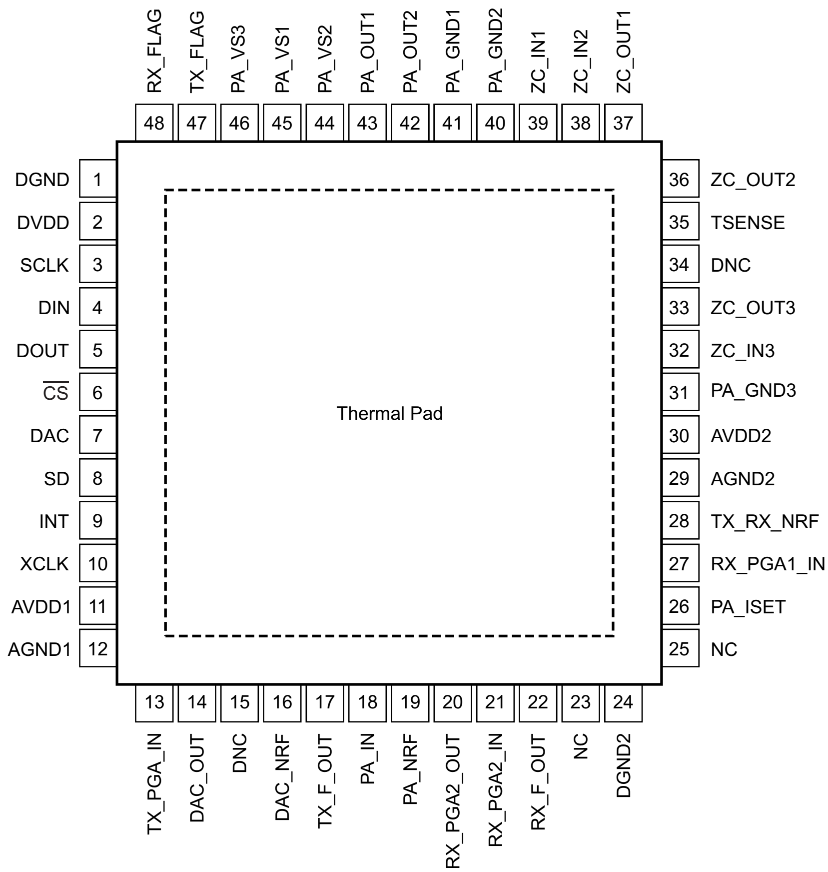


Figure 2. SPI Mode 1,1

PIN CONFIGURATION

RGZ PACKAGE
QFN-48
(TOP VIEW)

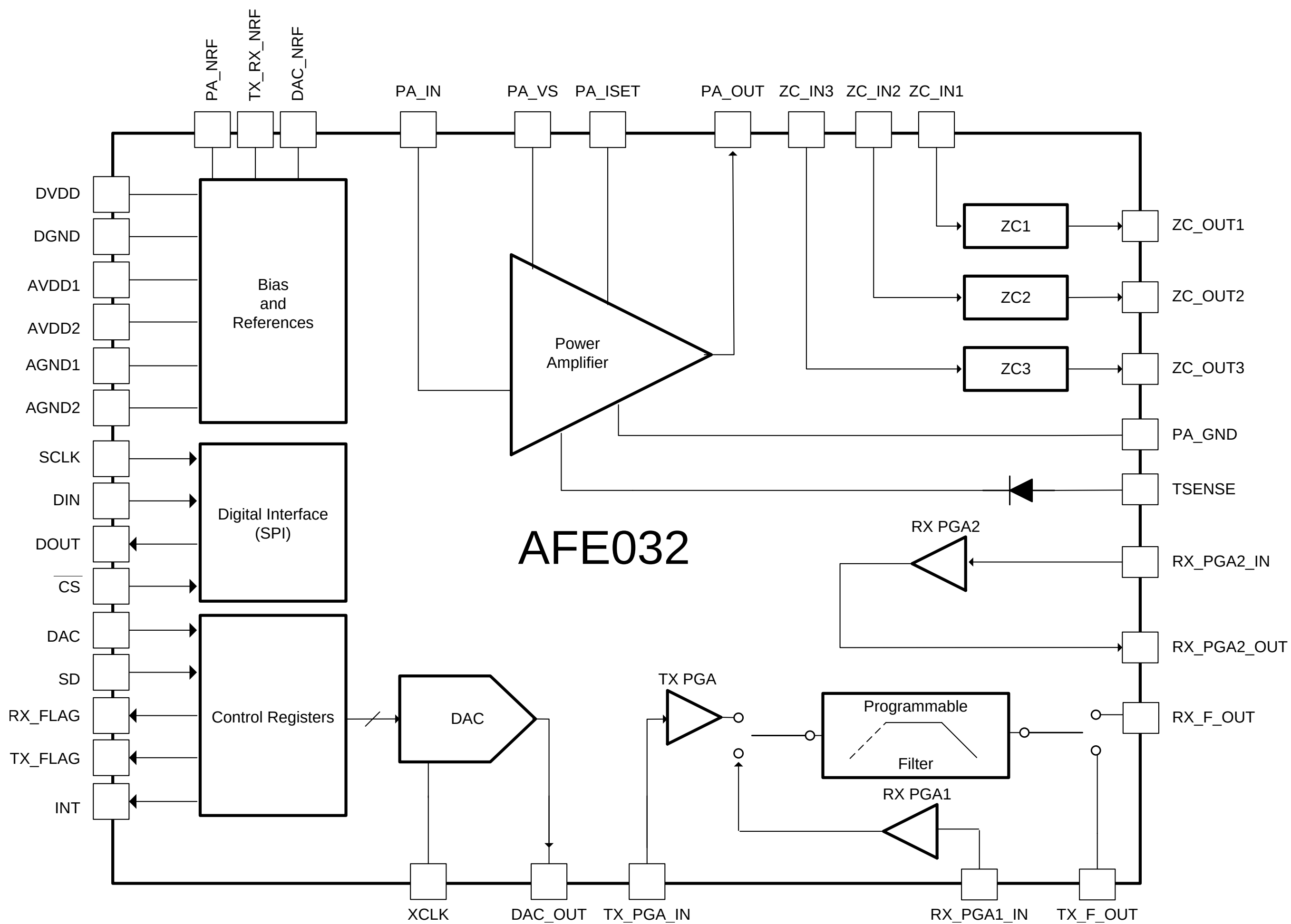


NOTE: Connect exposed thermal pad to ground.

PIN DESCRIPTIONS

NAME	PIN NO.	DESCRIPTION
AGND1	12	Analog ground
AGND2	29	Analog ground
AVDD1	11	Analog supply
AVDD2	30	Analog supply
$\overline{CS}$	6	SPI digital chip-select input
DAC	7	DAC mode select digital input
DAC_OUT	14	DAC analog output
DAC_NRF	16	DAC noise-reducing filter analog input
DGND	1	Digital ground
DGND2	24	Digital ground
DIN	4	SPI digital input
DNC	15, 34	Do not connect
DOUT	5	SPI digital output (push or pull)
DVDD	2	Digital supply
INT	9	Interrupt on undervoltage, undercurrent, or thermal overload (digital output, open-drain, active low)
NC	23, 25	No internal connection (connect to GND or leave unconnected)
PA_GND1	41	Power amplifier ground
PA_GND2	40	Power amplifier ground (connect to PA_GND1, pin 41)
PA_GND3	31	Power amplifier ground (connect to PA_GND1, pin 41)
PA_IN	18	Power amplifier analog input
PA_ISET	26	Power amplifier current-limit adjust pin (left open if not used)
PA_NRF	19	Power amplifier noise-reducing filter analog input
PA_OUT1	43	Power amplifier output
PA_OUT2	42	Power amplifier output (connect to PA_OUT1, pin 43)
PA_VS1	45	Power amplifier supply
PA_VS2	44	Power amplifier supply (connect to PA_VS1, pin 45)
PA_VS3	46	Power amplifier supply (connect to PA_VS1, pin 45)
RX_F_OUT	22	Receiver filter analog output
RX_FLAG	48	Receiver ready flag (digital output, open-drain, active low)
RX_PGA1_IN	27	Receiver PGA1 analog input
RX_PGA2_IN	21	Receiver PGA2 analog input
RX_PGA2_OUT	20	Receiver PGA2 analog output
SCLK	3	SPI serial clock input
SD	8	System shutdown digital input (active high)
TSENSE	35	Analog temperature sensing diode (anode)
TX_F_OUT	17	Transmit filter analog output
TX_FLAG	47	Transmitter ready flag (digital output, open-drain, active low)
TX_PGA_IN	13	Transmitter PGA analog input
TX_RX_NRF	28	Transmitter and receiver noise-reducing filter analog input
XCLK	10	DAC clock digital input
ZC_IN1	39	Zero-crossing detector 1, analog input
ZC_IN2	38	Zero-crossing detector 2, analog input
ZC_IN3	32	Zero-crossing detector 3, analog input
ZC_OUT1	37	Zero-crossing detector 1, digital output (push or pull)
ZC_OUT2	36	Zero-crossing detector 2, digital output (push or pull)
ZC_OUT3	33	Zero-crossing detector 3, digital output (push or pull)

FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

At T_J = +25°C, $V_{PA\ V\ S}$ = 15 V, and V_{AVDD} = V_{DVDD} = 3.3 V, unless otherwise noted.

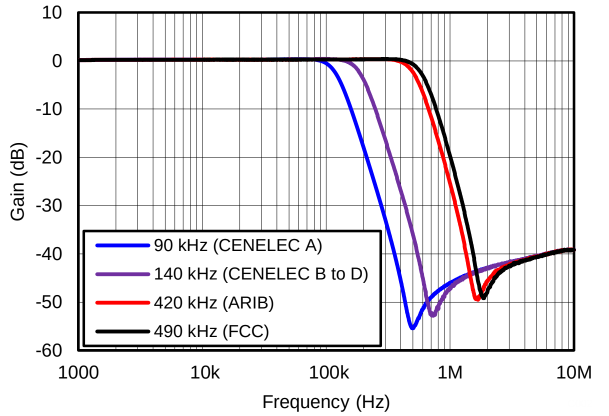


Figure 3. Tx, Rx LOW-PASS FILTER GAIN vs FREQUENCY

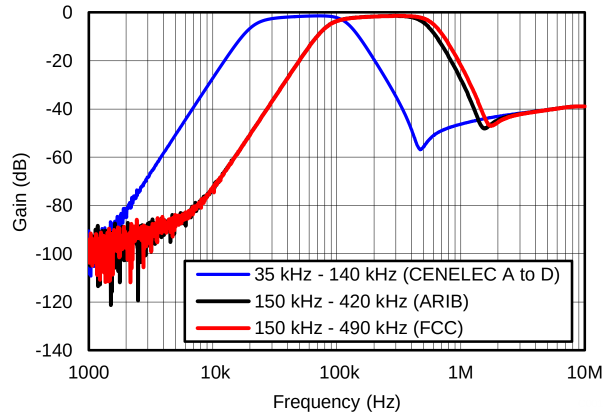


Figure 4. Rx BAND-PASS FILTER GAIN vs FREQUENCY

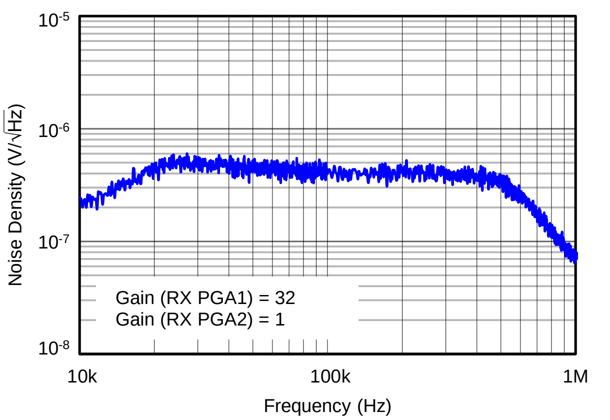


Figure 5. Rx PATH NOISE DENSITY

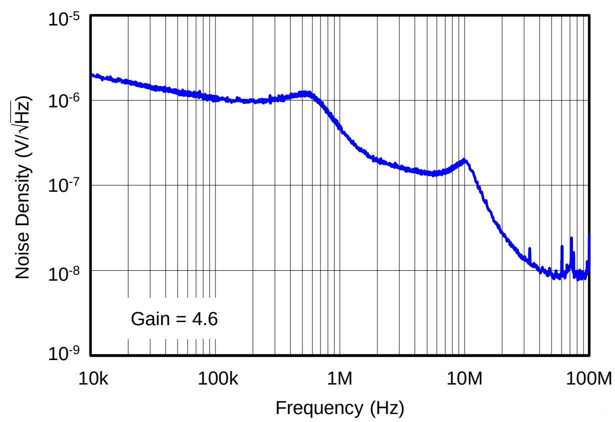


Figure 6. Tx PATH NOISE DENSITY

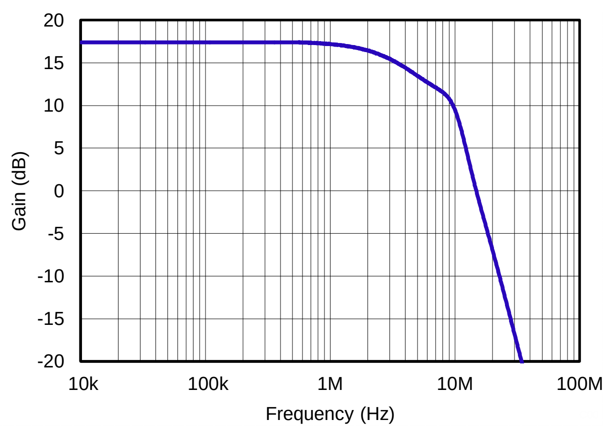


Figure 7. PA GAIN vs FREQUENCY

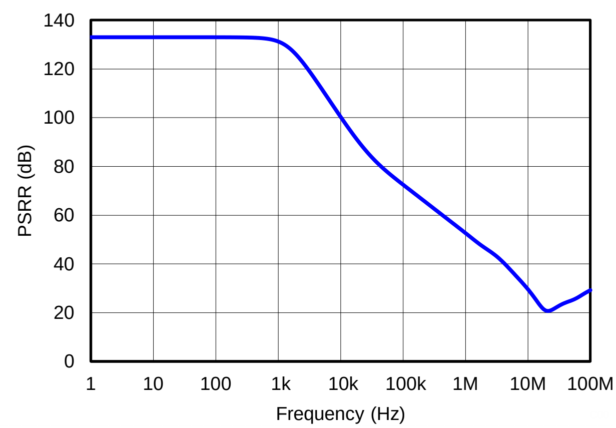


Figure 8. PA PSRR vs FREQUENCY

TYPICAL CHARACTERISTICS (continued)

At T_J = +25°C, $V_{PA\ V\ S}$ = 15 V, and V_{AVDD} = V_{DVDD} = 3.3 V, unless otherwise noted.

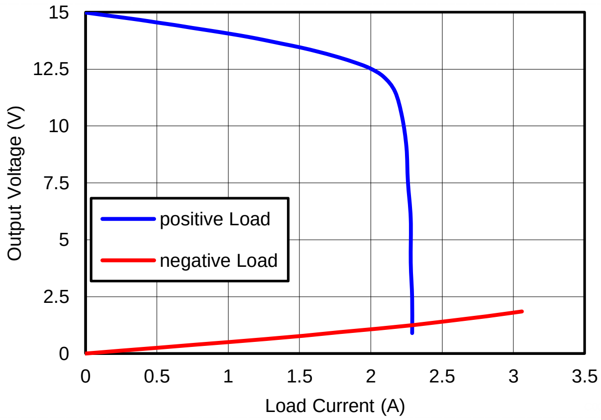


Figure 9. PA OUTPUT vs OUTPUT LOAD

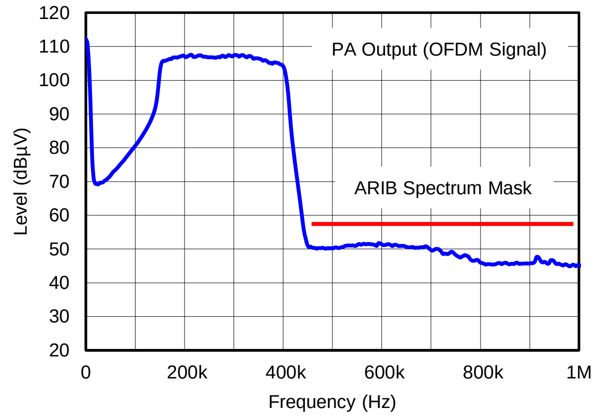


Figure 10. ARIB CONDUCTED EMISSIONS

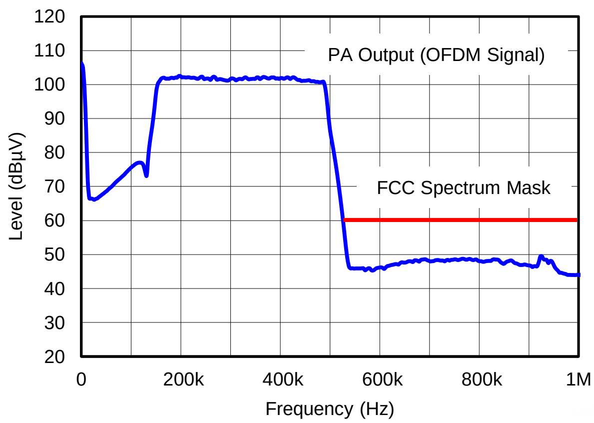


Figure 11. FCC CONDUCTED EMISSIONS

APPLICATION INFORMATION

GENERAL DESCRIPTION

The AFE032 is an integrated, power-line communication, analog front-end device that functions in conjunction with a microcontroller. The device conditions data generated in a microcontroller and transmits such data onto power lines through a line-coupling circuit.

The device includes several primary functional blocks:

- A power amplifier (PA) transmits data onto power lines through a line-coupling circuit.
- The transmit path (Tx) consists of a high-precision, digital-to-analog converter (DAC), programmable amplifier (TX_PGA), and low-pass filter (LPF).
- The receive path (Rx) consists of two programmable amplifiers (RX_PGA1 and RX_PAG2) and a band-pass filter [(an LPF and a high-pass filter (HPF)].

BLOCK DESCRIPTIONS

Power Amplifier Block

The power amplifier (PA) block consists of a high slew rate, high-voltage, and high-current operational amplifier. The PA is configured with an inverting gain of 7 V/V, has a low-pass filter response, and maintains excellent linearity and low distortion throughout its bandwidth. The PA is specified to operate from 7 V to 24 V and can deliver up to ±1.9 A of continuous output current over the specified junction temperature range of –40°C to +125°C. The PA block is shown in Figure 12.

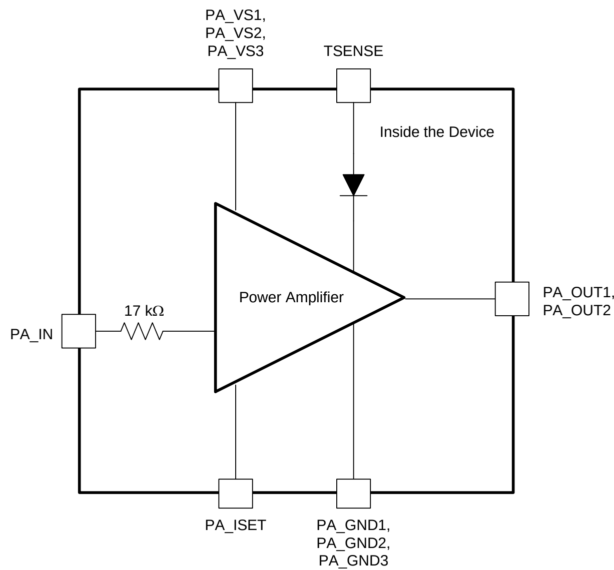


Figure 12. PA Block Equivalent Circuit

Connecting the PA in a typical power line communication (PLC) application requires few additional components. Figure 13 shows the typical connections to the PA block.

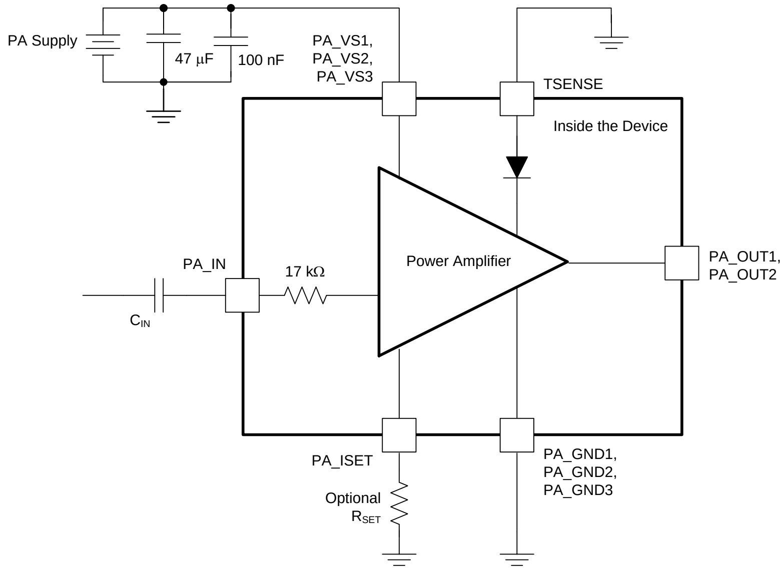


Figure 13. Typical Connections to the PA

The external capacitor (C_{IN}) introduces a single-pole, high-pass characteristic to the PA transfer function. The C_{IN} and PA combination has a band-pass response because of the inherent low-pass transfer function from the PA. The value of the high-pass cutoff frequency is determined by C_{IN} reacting with the input resistance of the PA circuit, and can be determined by Equation 1:

$$C_{IN} = \frac{1}{2 \times \pi \times 18\ k\Omega \times f_{HP}}$$

where:

- C_{IN} = external input capacitor and
- f_{HP} = desired high-pass cutoff frequency. (1)

For example, setting C_{IN} to 3.3 nF results in a high-pass cutoff frequency of 2.9 kHz. The voltage rating for C_{IN} should be determined to withstand operation up to the PA power-supply voltage.

When the transmitter is not in use, the output can be disabled and placed in a high-impedance state by following the procedure outlined in the *Power Amplifier Enable Sequence* section.

Refer to the *Initialization Sequence* and *Power Amplifier Enable Sequence* sections for details on the proper sequence when enabling the power amplifier.

PA Current Limiting

The PA_ISET pin (pin 26) provides a resistor-programmable output current limit for the PA block. Equation 2 determines the value of the external R_{SET} resistor attached to this pin.

$$I_{LIM} = \frac{1.2\ V \times 16.320\ k\Omega}{R_{INT} + R_{SET}} \tag{2}$$

where:

- R_{SET} = the value of the external resistor connected between pin 26 and ground,
- R_{INT} = the value of the internal resistor as programmed by the SPI interface in Table 18 (bits 4 and 5), and
- I_{lim} = the value of the desired current limit for the PA.

R_{INT} bit setting for bits 4 and 5 in Table 18 are listed in Table 1.

Table 1. R_{INT} Bit Settings

BIT SETTING	R_{INT} VALUE
00	17 kΩ
01	11 kΩ
10	8 kΩ
11	1.2 kΩ

Note that there is a 30% tolerance on the I_{lim} value given by Equation 2.

Tx Block

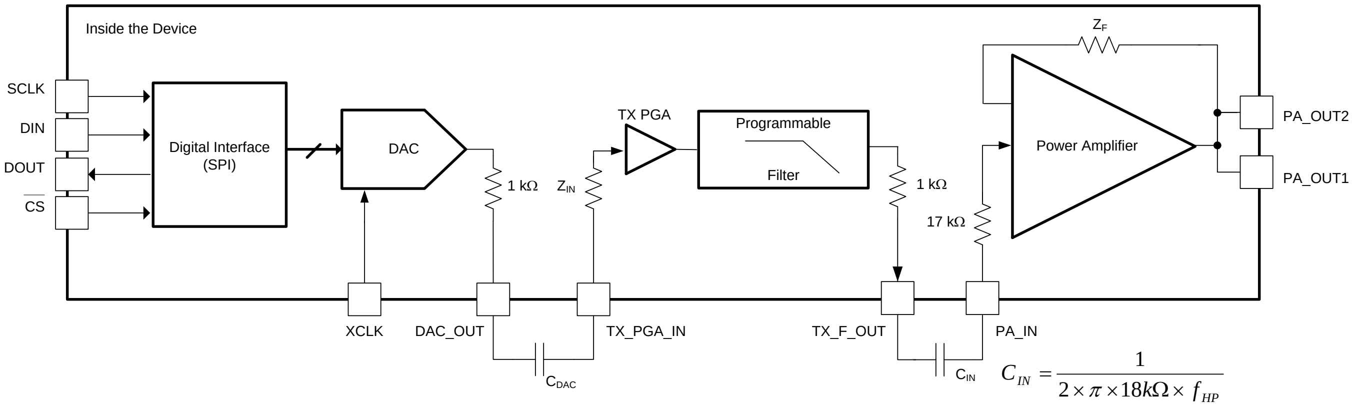
The Tx block consists of the Tx PGA and Tx filter.

The Tx PGA is a low-noise, high-performance, programmable gain amplifier. In DAC mode [where the DAC pin, pin 7, is a logic '1' and Tx enable (bit 4 in the REG_RX/TX_CTL register) is a logic '1'], the Tx PGA operates as the internal digital-to-analog converter (DAC) output buffer with programmable gain. The Tx PGA gain is programmed through the serial interface. The Tx PGA gain settings are 1.15 V/V, 2.3 V/V, 3.25 V/V, and 4.6 V/V. Gain is selectable via the TX_PGA gain pins (bits 2 to 0 in the REG_RX/TX_CTL register).

The Tx filter is a unity-gain, fourth-order, low-pass filter. The Tx filter cutoff frequency is selectable between the CENELEC (bands A, B, C, or D), ARIB, or FCC modes. The LPF band select bits (bits 6 to 4 in the REG_HPF/LPF_CFG register) determine the cutoff frequency.

When in DAC mode, the device accepts serial data from the microprocessor and writes that data to the internal DAC registers.

Proper connections for the Tx signal path for DAC mode operation are shown in Figure 14.



(1) For the capacitor value of C_{IN}, f_{HP} is the desired lower cutoff frequency and 17 kΩ is the PA input resistance.

Figure 14. Recommended Tx Signal Chain Connections

The capacitors listed in Figure 14 should be rated to withstand the full AVDD power-supply voltage for C_{DAC} and PA_VS for C_{IN}.

Rx Block

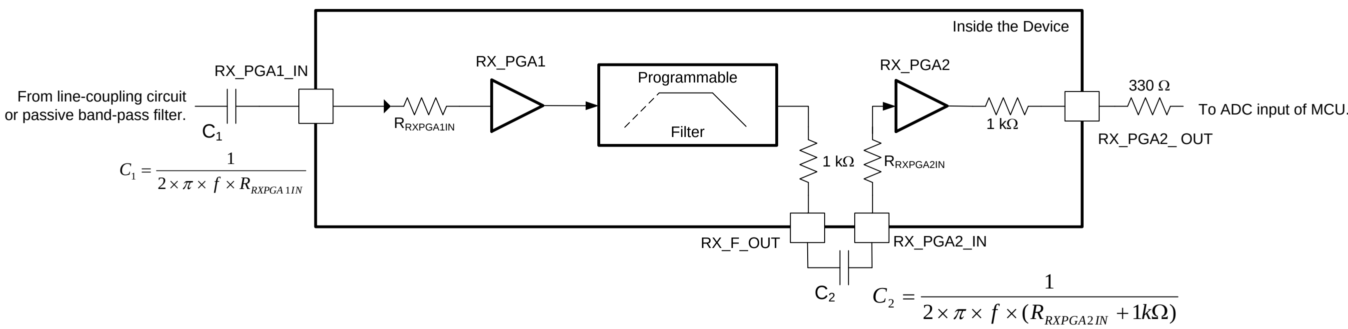
The Rx block consists of the Rx PGA1, Rx filter, and Rx PGA2. Both Rx PGA1 and Rx PGA2 are high-performance programmable gain amplifiers that can be configured through the SPI interface.

Rx PGA1 can operate as either an attenuator or in gain. The Rx PGA1 gain steps are 0.125 V/V, 0.25 V/V, 0.5 V/V, 1 V/V, 2 V/V, 4 V/V, 8 V/V, 16 V/V, and 32 V/V. Gains are selectable with the RX_PGA1 gain bits (bits 7 to 4 in the REG_RXPGA_CFG register). Configuring the Rx PGA1 as an attenuator (at gains less than 1 V/V) is useful for applications where large interference signals are present within the signal band. Attenuating the large interference allows these signals to pass through the analog Rx signal chain without causing an overload; the interference signal can then be processed and removed within the microprocessor as necessary. Similarly, if a transmitter is located close to the receiver, gains less than 1 V/V may be needed.

The Rx PGA2 gain steps are 1 V/V, 4 V/V, and 16 V/V. Gains are selectable through the RX_PGA2 gain bits (bits 3 to 1 in the REG_RXPGA_CFG register).

The Rx filter is a very low-noise, unity-gain, fourth-order, low-pass or band-pass filter. The Rx filter cutoff frequency is selectable between the CENELEC (bands A, B, C, or D), ARIB, or FCC modes. The LPF band select bits (bits 6 to 4 of the REG_HPF/LPF_REG register) determine the cutoff frequency for the LPF. The HPF band select bits (bits 1 and 2 of the REG_HPF/LPF_REG register) set up the cutoff frequency of the HPF.

Recommended connections for the Rx signal chain are shown in Figure 15.

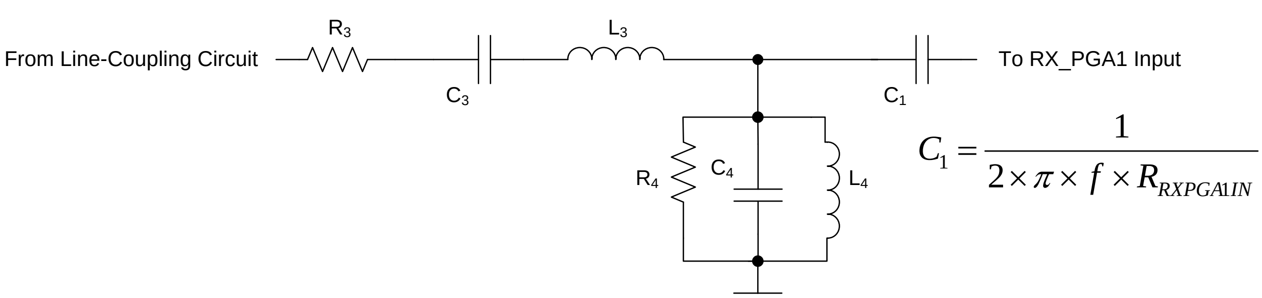


(1) For capacitor value C_1, f is the desired lower cutoff frequency and $R_{RXPAG1IN}$ is the input resistance of RX_PGA1.

(2) For capacitor value C_2, f is the desired lower cutoff frequency and $R_{RXPAG2IN}$ is the input resistance of RX_PGA2.

Figure 15. Recommended Connections for Rx Signal Chain

Figure 16 shows, a fourth-order, passive band-pass filter that is optional but recommended for applications with high performance needs. The external passive band-pass filter removes unwanted, out-of-band signals from the signal path, and it prevents such signals from reaching the active internal filters within the device.



(1) For capacitor value C_1, f is the desired lower cutoff frequency and $R_{RXPGA1IN}$ is the input resistance of RX_PGA1.

Figure 16. Passive Band-Pass Rx Filter

The following steps can be used to quickly design the passive pass-band filter. (Note that these steps produce an approximate result.)

1. Choose the filter characteristic impedance, Z_C:
   – For a –6-db passband attenuation: $R_3 = R_4 = Z_C$.
   – For a 0-db passband attenuation: $R_4 = Z_C$, $R_3 = 10 \times Z_C$.
2. Calculate values for C_3, C_4, L_3, and L_4 using the following equations:

$$C_3 = \frac{1}{2 \times \pi \times f_3 \times Z_C}$$

$$C_4 = \frac{1}{2 \times \pi \times f_4 \times Z_C}$$

$$L_3 = \frac{Z_C}{2 \times \pi \times f_3}$$

$$L_4 = \frac{Z_C}{2 \times \pi \times f_4}$$

Table 2 and Table 3 show standard values for common applications.

Table 2. Recommended Component Values for Fourth-Order Passive Band-Pass Filters (0-dB Pass-Band Attenuation)

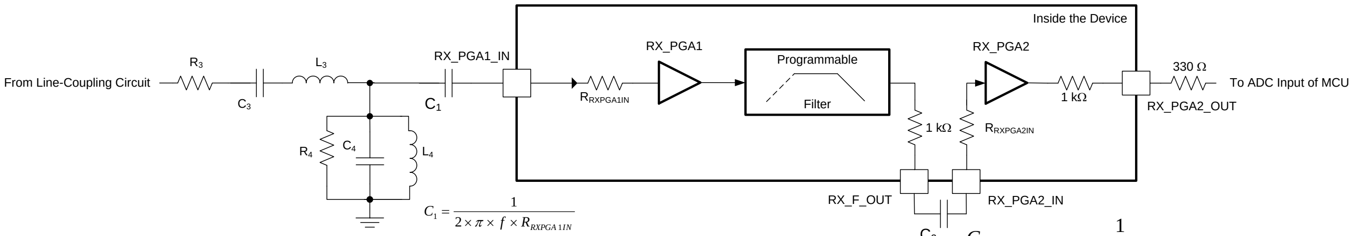
FREQUENCY BAND	FREQUENCY RANGE (kHz)	CHARACTERISTIC IMPEDANCE	R3	R4 (kΩ)	C3 (nF)	C4 (nF)	L3 (µH)	L4 (µH)
CENELEC A	35 to 95	1 kΩ	1 kΩ	10	4.7	1.5	1500	4700
CENELEC B, C, D	95 to 150	1 kΩ	1 kΩ	10	1.7	1	1200	1500
SFSK	63 to 74	1 kΩ	1 kΩ	10	2.7	2.2	2200	2200
FCC and ARIB	15 to 600	100 Ω	100 Ω	1	100	2.2	27	1000

Table 3. Recommended Component Values for Fourth-Order Passive Band-Pass Filters (–6-dB Pass-Band Attenuation)

FREQUENCY BAND	FREQUENCY RANGE (kHz)	CHARACTERISTIC IMPEDANCE	R3	R4	C3 (nF)	C4 (nF)	L3 (µH)	L4 (µH)
CENELEC A	35 to 95	1 kΩ	1 kΩ	1 kΩ	4.7	1.5	1500	4700
CENELEC B, C, D	95 to 150	1 kΩ	1 kΩ	1 kΩ	1.7	1	1200	1500
SFSK	63 to 74	1 kΩ	1 kΩ	1 kΩ	2.7	2.2	2200	2200
FCC and ARIB	15 to 600	100 Ω	100 Ω	100 Ω	100	2.2	27	1000

Avoid excessive capacitive loading when laying out the printed circuit board (PCB) traces from the inputs or outputs of the Rx block components. Keeping the PCB capacitance from the inputs to ground, or outputs to ground, below 100 pF is recommended.

Figure 17 shows the complete Rx signal path, including the optional passive band-pass filter.



$$C_1 = \frac{1}{2 \times \pi \times f \times R_{RXPGA1IN}}$$

$$C_2 = \frac{1}{2 \times \pi \times f \times (R_{RXPGA2IN} + 1k\Omega)}$$

(1) For capacitor value C_1, f is the desired lower cutoff frequency and $R_{RXPGA1IN}$ is the input resistance of RX_PGA1.

(2) For capacitor value C_2, f is the desired lower cutoff frequency and $R_{RXPGA2IN}$ is the input resistance of RX_PGA2.

Figure 17. Complete Rx Signal Path (with Optional Band-Pass Filter)

DAC Block and DSP Path

The AFE032 contains a digital signal processing (DSP) path that receives incoming DAC samples delivered from an external processor, conditions each sample, and delivers these samples to a 12-bit DAC. The device serial interface is used to write directly to the DSP path when the DAC pin (pin 7) is driven high. Use the following sequence to write samples to the DAC:

- Send a valid XCLK signal to the device (refer to the *AFE032 Clock Requirements* section for more details on the XCLK signal).
- Set $\overline{\text{CS}}$ low.
- Wait 20 DAC_CLK cycles (refer to the *AFE032 Clock Requirements* section for more details on the relationship between the XCLK frequency and DAC_CLK frequency).
- Set the DAC pin (pin 7) high to configure the device in DAC mode.
- Write a 12-bit word to DIN. (1) Note that the DAC register is left-justified.
- Set $\overline{\text{CS}}$ high to indicate that the sample is entered.

Refer to the *DAC Mode* section for more details on using the device in DAC mode.

The full-scale DAC output swing equals the DAC_NRF voltage level. Table Table 4 shows the ideal dc DAC output voltage for a given input code.

Table 4. Ideal DAC Output

INPUT CODE (Hex)	IDEAL DAC OUTPUT VOLTAGE (V)
7FF	DAC_NRF bias voltage
001	[(DAC_NRF bias voltage) / (2^{12} – 1)] + (DAC_NRF bias voltage) / 2
000	(DAC_NRF bias voltage) / 2
FFF	[(DAC_NRF bias voltage) / 2] – (DAC_NRF bias voltage) / (2^{12} – 1)
800	0

(1) The only exception to the 12-bit DAC sample length is when using a 16-bit envelope. See the *SPI Envelope Exception Case* section for more details.

DAC_NRF, PA_NRF, and TX_RX_NRF Blocks

The DAC_NRF, PA_NRF, and TX_RX_NRF blocks create biasing points used internally to the device. Each reference divides its respective power-supply voltage with a precision resistive voltage divider. PA_NRF provides a PA_VS / 2 voltage used for the PA; TX_RX_NRF provides an AVDD / 2 voltage used for the Tx PGA, Tx filter, Rx PGA1, Rx filter, and Rx PGA2; and DAC_NRF provides an AVDD / 4.7 voltage used for the DAC. Each NRF block has its output brought out to an external pin that can be used for filtering and noise reduction. These capacitors are optional, but are recommended for best performance.

Zero-Crossing Detector Block

The device includes three zero-crossing detectors. Zero-crossing detectors can be used to synchronize communications signals to the ac line or sources of noise. Typically, in single-phase applications, only a single zero-crossing detector is used. In three-phase applications, two or three zero-crossing detectors can be used. Figure 18 shows the AFE032 configured for non-isolated, zero-crossing detection.

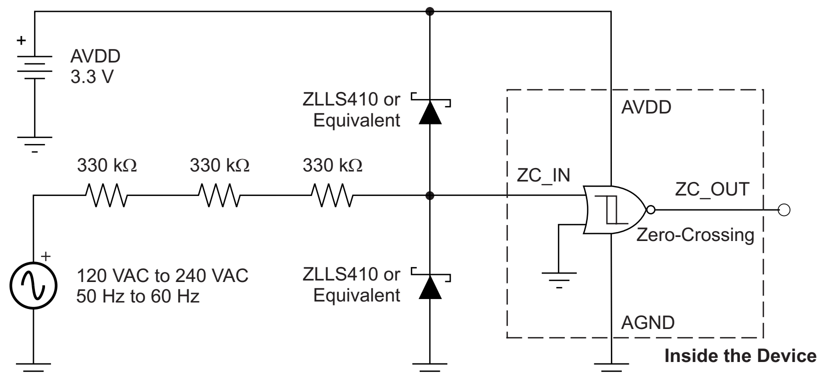


Figure 18. Non-Isolated Zero-Crossing Detection Using the AFE032

Non-isolated zero-crossing waveforms are shown in Figure 19.

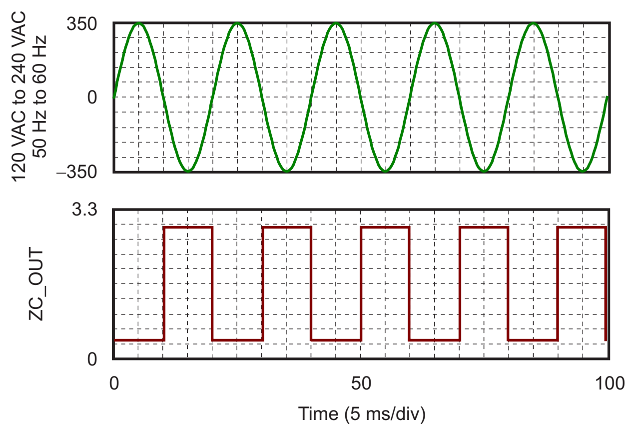


Figure 19. Non-Isolated, Zero-Crossing Waveforms

Schottky diodes are recommended (see Figure 18) for maximum device protection from line transients. These diodes limit the ZC_IN pins (pins 32, 38, and 39) to within the maximum rating of (AVDD + 0.4 V) and (AGND – 0.4 V). Some applications may require an isolated zero-crossing detection circuit. With a minimal amount of components, the AFE032 can be configured for isolated zero-crossing detection, as shown in Figure 20.

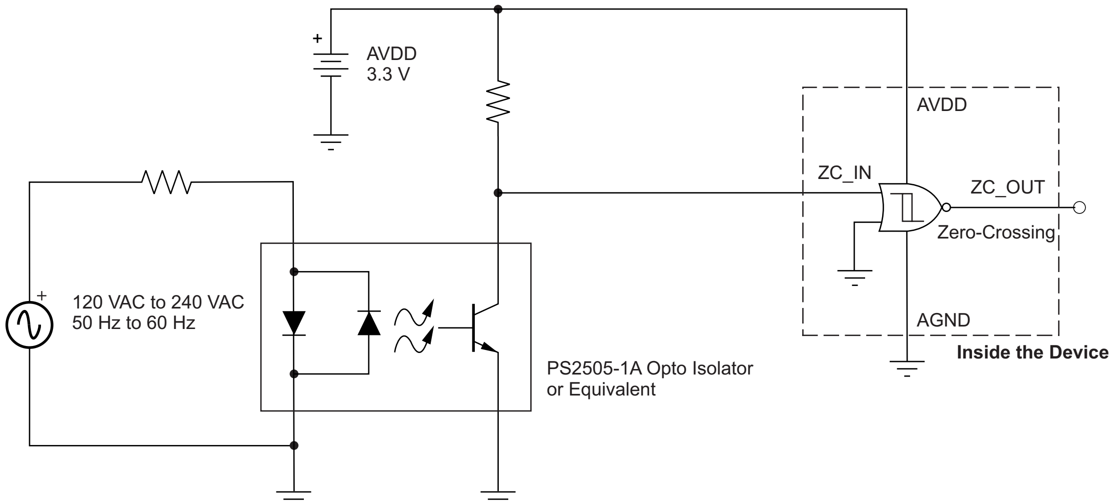


Figure 20. Isolated Zero-Crossing Detection Using the AFE032

Isolated zero-crossing waveforms are shown in Figure 21.

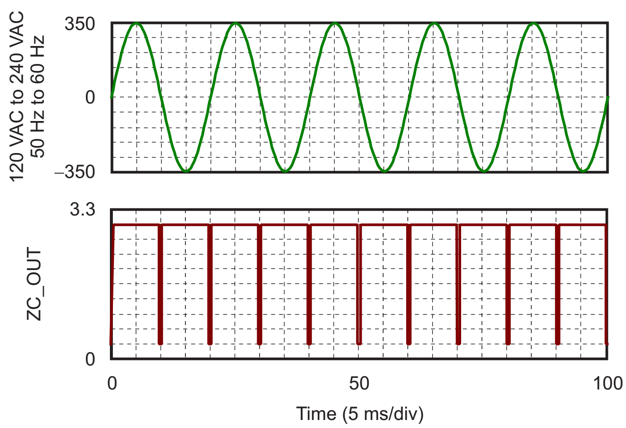


Figure 21. Isolated Zero-Crossing Waveforms

DIGITAL LOGIC INTERFACE

The primary functions of the AFE032 digital module are to:

- Provide an interface for an external DSP to configure the internal blocks of the AFE032.
- Provide a digital processing path that conditions samples coming from an external DSP.
- Transmit the conditioned samples to the internal 12-bit DAC.

To accomplish these functions, the device digital logic supports two modes of operation: SPI mode and DAC mode.

In SPI mode, the device processes commands to either configure the internal analog and digital circuits or to provide status to an external DSP. In DAC mode, an external DSP uses the SPI to provide DAC samples to the device.

Descriptions of all the registers mentioned in this section can be found in the *Register Map* section.

AFE032 Clock Requirements

The device requires the following clocks: XCLK and SCLK.

XCLK is a free-running clock with a 50/50 duty cycle, frequency ranges from 10 MHz to 40 MHz, and less than 180 ps of RMS jitter. SCLK is an SPI clock used for the SPI interface with frequency ranges from 14 MHz to 30 MHz. This clock is active when $\overline{CS}$ is '0'.

The device contains two programmable clock dividers that can be used to generate the internal DAC clock (referred to as *DAC_CLK*). This internal DAC clock determines the rate at which the internal device DAC updates its analog output. The internal DAC clock is also used by the digital logic in the device (with the exception of the SPI slave module that requires a separate SCLK signal). The REG_CLK_DIV register is programmed by the user to control the internal DAC clock frequency. The internal DAC clock is created by two 4-bit clock dividers in series. Each divider is a 4-bit decimal clock divider that can divide the frequency of the XCLK signal by an integer between 1 and 16. Each clock divider produces an N+1 divided-down clock, where *N* is the programmed, 4-bit divide value. The XCLK frequency can be divided by a maximum value of 256. The first divider in the series is controlled by the POST_CLK_DIV bits (bits 7 to 4 in the REG_CLK_DIV register) and the second divider is controlled by the PRE_CLK_DIV bits (bits 3 to 0 in the REG_CLK_DIV register). If the application does not need to divide XCLK by a value greater than 16, then POST_CLK_DIV is not programmed because these bits default to '0'. For applications where XCLK must be divided down by a number greater than 16, both PRE_CLK_DIV and POST_CLK_DIV are used to create the target divide-down value required to generate DAC_CLK. In sum, the relationship between XCLK and DAC_CLK can be expressed as Equation 3:

$$XCLK = (POST\_CLK\_DIV + 1)\,(PRE\_CLK\_DIV + 1)\,(DAC\_CLK) \quad (3)$$

Note that for proper device operation, DAC_CLK must always be slower than SCLK.

In DAC mode, an external processor (also referred to as the *SPI master* or *external DSP*) transmits DAC samples to the device via the SPI at a rate of f_S samples per second. f_S may be less than or equal to DAC_CLK; however, the external processor clock and the AFE032 XCLK must be generated from the same crystal.

Power-Up Sequence

A specific power-up sequence must be implemented to properly use the AFE032. The device internal blocks are disabled if proper VDD levels are not maintained. The following sequence applies at power-up (note that the SD pin must be held low throughout the entire power-up sequence):

- Power is applied to the device.
- When the supply connected to the AVDD1, AVDD2, and DVDD pins reaches a valid, 3-V dc voltage level, the device digital logic comes out of reset.
- At this point, a valid XCLK signal is sent to the device for at least 65,536 cycles.

Every time power is applied to the device, in addition to the power-up sequence, a complete initialization sequence must be followed before the user can transmit data with the power amplifier. The complete initialization sequence must be followed also after a soft reset is performed (see the AFE032 Reset Options section for more information on soft reset). The *Initialization Sequence* section provides more details. Similarly, perform a sequence each time the device transitions from receiver mode (also referred to as *RX mode*) to transmitter mode (also referred to as *TX mode*). The *Power Amplifier Enable Sequence* section provides more details for this Rx to Tx mode transition sequence.

SPI Mode

Holding the DAC pin low places the device in SPI mode. The following rules apply to the SPI slave operation when the device is in SPI mode:

- Each SPI operation is 16 bits wide.
- The $\overline{CS}$ pin is set to '0' for each 16-bit SPI operation.
- The $\overline{CS}$ pin is set to '1' between consecutive SPI operations.
- A minimum of ten DAC_CLK cycles must be inserted after a write operation and a minimum of five DAC_CLK cycles must be inserted after a read operation. During these cycles, the $\overline{CS}$ pin is set to '1'.
- The device DIN pin value is latched in during the SCLK rising edge.
- The device drives DOUT on the SCLK falling edge.
- DOUT assumes a high-impedance state when $\overline{CS}$ is set to '1'.

During an SPI operation in SPI mode, the following protocol is applied to the DIN pin by the SPI master:

- The first bit of the operation is the read and write (R/W) bit. An SPI read is specified when an R/W bit is '1'. An SPI write is specified when an R/W bit is '0'.
- The next seven bits are the SPI address.
- The next eight bits are the SPI data.

Table 5 lists a complete example of the 16-bit codeword format.

Table 5. 16-Bit Codeword Format for an SPI Operation in SPI Mode

BIT NAME	LOCATION (0 = LSB, 15 = MSB)	FUNCTION
DATA0	0	LSB of SPI data
DATA1	1	SPI data
DATA2	2	SPI data
DATA3	3	SPI data
DATA4	4	SPI data
DATA5	5	SPI data
DATA6	6	SPI data
DATA7	7	MSB of SPI data
ADDR0	8	LSB of register address bit
ADDR1	9	Register address bit
ADDR2	10	Register address bit
ADDR3	11	Register address bit
ADDR4	12	Register address bit
ADDR5	13	Register address bit
ADDR6	14	MSB of register address bit
R/W	15	Read or write: 0 = write, 1 = read

During an SPI operation, the following protocol is applied to the DOUT pin:

- If the current SPI operation from the master is a write operation, the AFE032 displays the previous operation received from the master on DOUT.
- If the current SPI operation from the master is a read operation, the AFE032 displays the R/W bit of the previous operation followed by the 7-bit address of the previous operation on DOUT. The remaining eight bits that follow depend on whether the previous operation was a read or write operation.
  - If a read request immediately follows a write operation, then the last eight bits are whatever was written to the device on DIN by the SPI master.
  - If a read request immediately follows a read operation, then the last eight bits are the contents of the AFE032 address used in the previous read operation.

Note that two SPI operations are required for the device to transmit status bits over the SPI. The first operation provides the AFE032 with the SPI register address to be read. The second operation transfers the data.

A minimum of ten DAC_CLK cycles must be inserted between consecutive write operations and a minimum of five DAC_CLK cycles must be inserted between consecutive read operations.

DAC Mode

The device digital logic contains four digital processing blocks to condition incoming DAC samples delivered from an external processor. The digital processing blocks in the device are referred to as the *DSP path*, as shown in Figure 22.

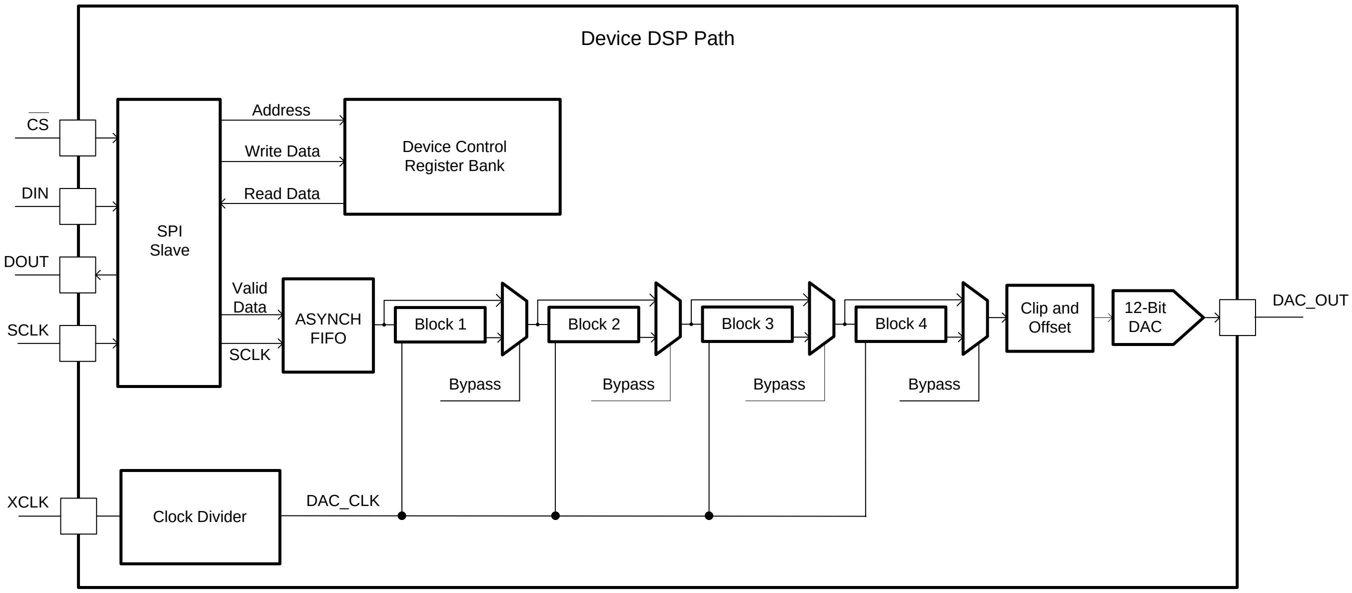


Figure 22. AFE032 DSP Path

Each block in the DSP path can be enabled or disabled to accommodate for different application scenarios. Processing DAC samples through the device can be broken down as follows:

- The device receives DAC samples (12 bits per sample) from an external DSP through the SPI at a rate of f_S samples per second.
- The device receives the 12-bit samples and processes them as real signed numbers. Thus, bit 11 is processed as a sign bit. Therefore, the absolute value of each sample has 11 bits of resolution.
- The device extracts the DAC samples from the SPI and synchronizes them to DAC_CLK through the ASYNCH FIFO.

NOTE

The only exception to the 12-bit DAC sample length is when using a 16-bit envelope. See the *SPI Envelope Exception Case* section for more details.

When an external DSP is ready to send DAC samples to the device, the DAC_MODE pin is asserted. The device digital logic reconfigures the SPI slave to run in a proprietary mode of operation in order to receive samples from the external DSP. In other words, the SPI interface becomes a write-only serial interface so that the external DSP can send DAC samples to the device. Each sample must be 12 bits wide.

The device digital logic sends valid samples to the DAC as long as the external DSP asserts the DAC_MODE pin and sends 12-bit samples to the device. Note that whenever DAC_MODE is not asserted, whichever values are present in the output stage of the DSP path continue to be driven to the DAC. Note also that, by default, all digital processing blocks in the device retain their states when DAC mode is deasserted (see the *DSP Path State Retention* section for more details). Use the following sequence to write samples to the DAC:

1. Send a valid XCLK signal to the device (refer to the *AFE032 Clock Requirements* section for more details on the XCLK signal).
2. Set $\overline{CS}$ low.
3. Wait for at least 20 DAC_CLK cycles.
4. Set DAC (pin 7) high. This setting places the device in DAC mode.
5. Write the first 12-bit word to DIN. Note that the DAC register is left-justified.
6. Set $\overline{CS}$ high to indicate that the sample is entered.
7. Wait for at least four SCLK cycles.
8. Set $\overline{CS}$ low.
9. Write the subsequent 12-bit word to DIN. Note that the DAC register is left-justified.
10. Set $\overline{CS}$ high for at least four SCLK cycles to indicate that the sample is entered.
11. Repeat the last three steps for each new DAC sample.

NOTE

The only exception to the 12-bit DAC sample length is when using a 16-bit envelope. See the *SPI Envelope Exception Case* section for more details.

Appending 24 mid-range value samples at the end of every transmission of DAC samples is recommended. These 24 samples provide a smooth transition of the entire transmit path (that is, DSP blocks, Tx PGA, and Tx filter) to SPI mode. When the transmission of the last DAC sample ends (and the $\overline{CS}$ pin is set high), wait for at least 20 DAC_CLK cycles before bringing the DAC pin (pin 7) low.

SPI Envelope Exception Case

Some external processors cannot create a 12-bit wide SPI transmission and output 16 bits. If this limitation is encountered, the device supports a special mode where a 12-bit DAC sample can be sent over the SPI inside a 16-bit window. To use the AFE032 16-bit SPI envelope feature take into account the following points:

- Set the DAC SPI select bit (bit 0 of the REG_AFE032_CTRL register) to '1'.
- Wait for at least 20 DAC_CLK cycles after setting the DAC SPI select bit.
- Set the DAC pin (pin 7) high. This setting places the device in DAC mode.
- Drive the 12-bit DAC sample in the MSB position of the 16-bit SPI envelope.
- Provide 16 valid SCLK cycles in the SPI envelope.

The AFE032 SPI slave latches the first 12 bits and forwards them to the DSP path. The remaining four bits are dropped. When operating the device with the 16-bit SPI envelope enabled, the SPI must be driven exactly as described in this section or the device will not process the DAC samples successfully.

Digital Filtering

Blocks 1 and 2 of the DSP path provide digital filtering to the samples generated by the external processor.

This section provides recommendations for the coefficient values for filter block 1 and filter block 2 of the DSP path. Three frequency bands are considered:

- CENELEC A band, comprised of frequencies between 3 kHz and 95 kHz.
- ARIB band, comprised of frequencies between 10 kHz and 450 kHz.
- FCC band, comprised of frequencies between 10 kHz and 490 kHz.

Note that the addresses of all registers mentioned in this section are given in the REGISTER MAP section.

Table 6 provides the recommended PRE_CLK_DIV and POST_CLK_DIV values of the REG_CLK_DIV register for the case of a 37.5 MHz XCLK frequency.

Table 6. Recommended Clock Divider Values for Different Frequency Bands and XCLK = 37.5 MHz

Frequency band	Clock divider value (decimal)	POST_CLK_DIV (Hex)	PRE_CLK_DIV (Hex)
CENELEC A	22	10	1
ARIB	7	0	6
FCC	7	0	6

Table 7 provides the recommended coefficient values (in hexadecimal form) for block 1.

Table 7. Recommended Coefficient Values for Block 1 of DSP Path

Register	CENELEC A	ARIB	FCC
REG_COEFF1_BLOCK_1_MS	Disable	CC	A3
REG_COEFF1_BLOCK_1_LS	Disable	40	E0
REG_COEFF2_BLOCK_1_MS	Disable	E4	D8
REG_COEFF2_BLOCK_1_LS	Disable	50	E0
REG_COEFF3_BLOCK_1_MS	Disable	40	40
REG_COEFF3_BLOCK_1_LS	Disable	00	00
REG_COEFF4_BLOCK_1_MS	Disable	78	7E
REG_COEFF4_BLOCK_1_LS	Disable	40	80
REG_COEFF5_BLOCK_1_MS	Disable	40	40
REG_COEFF5_BLOCK_1_LS	Disable	00	00
REG_COEFF6_BLOCK_1_MS	Disable	30	17
REG_COEFF6_BLOCK_1_LS	Disable	C0	A0
REG_COEFF7_BLOCK_1_MS	Disable	15	3E
REG_COEFF7_BLOCK_1_LS	Disable	A0	D0

Table 8 provides the recommended coefficient values (in hexadecimal form) for block 2.

Table 8. Recommended Coefficient Values for Block 2 of DSP Path

Register	CENELEC A	ARIB	FCC
REG_COEFF1_BLOCK_2_MS	10	F8	D4
REG_COEFF1_BLOCK_2_LS	40	30	00
REG_COEFF2_BLOCK_2_MS	00	00	00
REG_COEFF2_BLOCK_2_LS	00	00	00
REG_COEFF3_BLOCK_2_MS	0C	0C	0C
REG_COEFF3_BLOCK_2_LS	F0	B0	60
REG_COEFF4_BLOCK_2_MS	0C	0C	0C
REG_COEFF4_BLOCK_2_LS	F0	B0	60
REG_COEFF5_BLOCK_2_MS	00	00	00
REG_COEFF5_BLOCK_2_LS	00	00	00
REG_COEFF6_BLOCK_2_MS	06	C3	96
REG_COEFF6_BLOCK_2_LS	E0	80	20
REG_COEFF7_BLOCK_2_MS	D1	D0	CC
REG_COEFF7_BLOCK_2_LS	80	F0	70
REG_COEFF8_BLOCK_2_MS	0A	09	19
REG_COEFF8_BLOCK_2_LS	C0	20	A0
REG_COEFF9_BLOCK_2_MS	06	0D	30
REG_COEFF9_BLOCK_2_LS	00	C0	E0
REG_COEFF10_BLOCK_2_MS	0A	09	19
REG_COEFF10_BLOCK_2_LS	C0	20	A0
REG_COEFF11_BLOCK_2_MS	2D	60	3B
REG_COEFF11_BLOCK_2_LS	20	60	C0
REG_COEFF12_BLOCK_2_MS	69	6B	6E
REG_COEFF12_BLOCK_2_LS	60	90	80

Figure 23 shows the transfer function of block 2 when the recommended coefficients for the CENELEC A band are used.

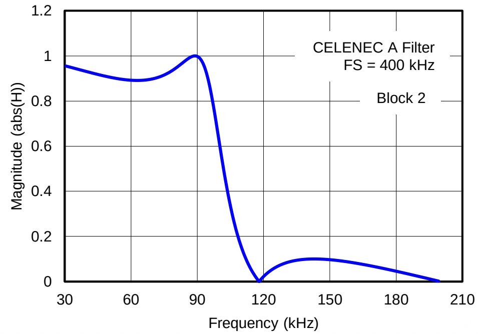


Figure 23. Transfer Function of Block 2 - CENELEC A Band Coefficients According to Table 8

Figure 24 shows the transfer function of blocks 1 and 2 when the recommended coefficients for the ARIB band are used.

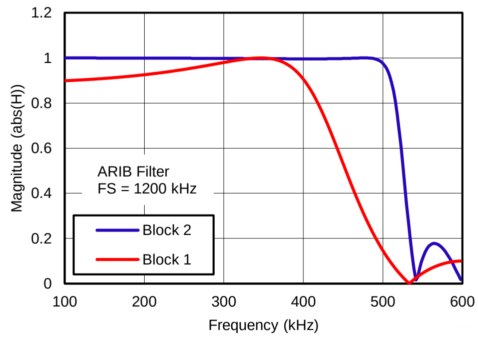


Figure 24. Transfer Function of Blocks 1 and 2 - ARIB Band Coefficients According to Table 7 and Table 8

Figure 25 shows the transfer function of blocks 1 and 2 when the recommended coefficients for the FCC band are used.

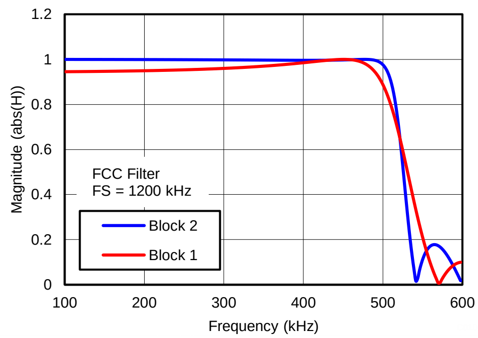


Figure 25. Transfer Function of Blocks 1 and 2 - FCC Band Coefficients According to Table 7 and Table 8

SPI Clock To DAC Clock Synchronization

The device receives DAC samples from the external DSP over the SPI (which operates using SCLK) and writes these samples to the ASYNCH FIFO for internal synchronization (the ASYNCH FIFO and the rest of the DSP path operate using the internally-generated DAC_CLK signal). The FIFO read controller pulls the samples out of the ASYNCH FIFO at the rate determined by the DAC_CLK frequency (not the rate determined by f_S).

Refer to Figure 22 for the block diagram of the AFE032 DSP path. Bits 1 though 4 of the REG_AFE032_CTRL register determine which blocks are included in the DSP path and which are bypassed. The default values of these bits is '0' and all four blocks are included in the DSP path when the device is powered up.

Block 3 of the DSP path operates synchronously with DAC_CLK and interpolates (by a factor of four) the signals coming from the ASYNCH FIFO. Such interpolation requires that samples stored in the ASYNCH FIFO be extracted no faster than one time every four DAC_CLK cycles; such interpolation also imposes an upper bound to f_S. The external DSP must send samples to the device at a rate less than or equal to one-fourth the DAC_CLK frequency [that is, $f_S \leq$ (DAC_CLK / 4)].

Block 4 should be used to improve performance in two cases:

- When block 3 is included in the DSP path and f_S is strictly less than one-fourth the DAC_CLK frequency [that is, $f_S <$ (DAC_CLK / 4)].
- When block 3 is bypassed (not included in the DSP path) and f_S is strictly less than the DAC_CLK frequency (that is, $f_S <$ DAC_CLK).

For these two cases, block 4 should be used and its 32-bit parameter should be written to the REG_OFFSET0, REG_OFFSET1, REG_OFFSET2, and REG_OFFSET3 registers. This section describes four typical scenarios that can be found in most applications.

Block 3 and Block 4 Are Bypassed

If an external DSP transmits DAC samples to the device at a rate equal to the DAC_CLK frequency (that is, f_S = DAC_CLK), then both block 3 and block 4 should be bypassed. Write a '0' to bits 1 to 4 of the REG_AFE032_CTRL register. A parameter for block 4 does not need to be calculated or written. Table 9 shows examples of this scenario.

Table 9. Example Cases of Bypassed Blocks 3 and 4

f_S (kSPS)	XCLK (MHz)	XCLK DIVIDER	REG_CLK_DIV (Hex)	DAC_CLK (MHz)	BLOCK 3	BLOCK 4
500	37.5	75	4E	0.5	Bypassed	Bypassed
800	19.2	24	27	0.8	Bypassed	Bypassed

Block 3 Is Included, Block 4 Is Bypassed

If an external DSP transmits DAC samples to the device at a rate equal to one-fourth the DAC_CLK frequency [that is, f_S = (DAC_CLK / 4)], then block 3 is included and block 4 is bypassed. Write a '0' to bits 1, 2, and 4 and write a '1' to bit 3 of the REG_AFE032_CTRL register. A parameter for block 4 does not need to be calculated or written. Table 10 shows examples of this scenario.

Table 10. Example Cases of Block 3 Included and Block 4 Bypassed

f_S (MSPS)	XCLK (MHz)	XCLK DIVIDER	REG_CLK_DIV (Hex)	DAC_CLK (MHz)	BLOCK 3	BLOCK 4
1.2	19.2	4	03	4.8	Included	Bypassed
0.625	37.5	15	0E	2.5	Included	Bypassed

Block 3 Is Bypassed, Block 4 Is Included

If an external DSP transmits DAC samples to the device at a rate close to but less than the DAC_CLK frequency (that is, f_S < DAC_CLK), then block 3 is bypassed and block 4 is included. Write a '0' to bits 1, 2, and 3 and write a '1' to bit 4 of the REG_AFE032_CTRL register. In this case, the 32-bit parameter for block 4 must be calculated and written. This mode of operation is recommended as long as the ratio between f_S and DAC_CLK is greater than 0.8 and less than 1 (that is, 0.8 DAC_CLK < f_S < DAC_CLK). Table 11 shows examples of this scenario.

To calculate the 32-bit parameter for block 4:

- Calculate the ratio between f_S and DAC_CLK. Ratio = f_S / DAC_CLK.
- Multiply the ratio by 4,294,967,296. Product = (ratio)(4,294,967,296).
- The parameter for block 4 is equal to the integer part of the product found. Parameter = integer part of product.

The value of the 32-bit parameter for block 4 must be written in hexadecimal form to the REG_OFFSET0, REG_OFFSET1, REG_OFFSET2, and REG_OFFSET3 registers. The order should be such that the most significant byte of the parameter is stored in REG_OFFSET0 and the least significant byte is stored in REG_OFFSET3.

Table 11. Example Cases of Block 3 Bypassed and Block 4 Included

f_S (MSPS)	XCLK (MHz)	XCLK DIVIDER	REG_CLK_ DIV (Hex)	DAC_CLK (MHz)	BLOCK 3	BLOCK 4	BLOCK 4 PARAMETER (Hex)
1.2	37.5	28	1D	1.339	Bypassed	Included	E5604189
0.8	37.5	45	48	0.833	Bypassed	Included	F5C28F5C

Block 3 and Block 4 Are Included

If an external DSP transmits DAC samples to the device at a rate close to but less than one-fourth the DAC_CLK frequency [that is, f_S < (DAC_CLK / 4)], then both block 3 and block 4 are included. Write a '0' to bits 1 and 2 and write a '1' to bits 3 and 4 of the REG_AFE032_CTRL register. In this case, the 32-bit parameter for block 4 must be calculated and written. This mode of operation is recommended as long as the ratio between f_S and DAC_CLK is greater than 0.2 and less than 0.25 (that is, 0.2 DAC_CLK < f_S < 0.25 DAC_CLK). Table 12 shows examples of this scenario.

To calculate the 32-bit parameter for block 4:

- Calculate the ratio between f_S and DAC_CLK. Ratio = f_S / DAC_CLK.
- Multiply the ratio by 17,179,869,184. Product = (ratio)(17,179,869,184).
- The parameter for block 4 is equal to the integer part of the product found. Parameter = integer part of product.

The value of the 32-bit parameter for block 4 must be written in hexadecimal form to the REG_OFFSET0, REG_OFFSET1, REG_OFFSET2, and REG_OFFSET3 registers. The order should be such that the most significant byte of the parameter is stored in REG_OFFSET0 and the least significant byte is stored in REG_OFFSET3.

Table 12. Example Cases of Block 3 and Block 4 Included

f_S (MSPS)	XCLK (MHz)	XCLK DIVIDER	REG_CLK_ DIV (Hex)	DAC_CLK (MHz)	BLOCK 3	BLOCK 4	BLOCK 4 PARAMETER (Hex)
1	37.5	9	08	4.167	Included	Included	F5C28F5C
1	19.2	4	03	4.8	Included	Included	D5555555
0.4	22.5	14	0D	1.607	Included	Included	FEDCBA98

DSP Path State Retention

By default, blocks 1 through 4 of the DSP path retain their states in between DAC sample bursts (when DAC mode is deasserted). This default implementation functions best for most applications provided that all DAC sample bursts end with at least 24 samples of midrange values. These 24 samples provide a smooth transition to SPI mode. The default implementation can be altered by changing the DSP_CFG bit of the REG_AUX_CTL register (see the *Register Map* section).

DAC Sample Clipping and Bias

The device provides the ability to clip DAC samples at the last stage of digital processing. An additional offset may be added to the clipped DAC sample at the user's discretion. The clipping circuit operates in the following manner:

- Program the device with an 11-bit clip value on the REG_CLIP0 and REG_CLIP1 registers.
- Program the device with an 11-bit clip offset value on the REG_CLIP_OFFSET0 and REG_CLIP_OFFSET1 registers.
- The programmed clip and offset values are not signed.
- The device digital logic compares the 11-bit magnitude of the DAC sample from the DSP path to the clip value.
- If the magnitude of the DAC sample is greater than the clip value, then the final DAC sample equals the clip value minus the offset value.
- If the magnitude of the DAC sample is less than the clip value, then the final DAC sample is unchanged.

AFE032 Reset Options

The device has two main types of reset mechanisms available. These reset options are hardware invoked and software invoked.

External Reset and Analog Shutdown Mode

The device can be disabled by asserting the external SD pin. Asserting the external SD pin causes the device digital logic to reset and also causes the analog module to shut down. Asserting the external SD pin disables the DAC clock and the entire device is disabled. Adhere to the following protocol when asserting the external SD pin:

- Assert the SD pin for at least 1 µs.
- Make sure that the device receives a valid XCLK clock before, during, and after the SD pin is asserted.

When the SD pin is deasserted, a valid XCLK signal must be sent to the device for at least 65,536 cycles. The device must be reprogrammed because all control registers are now reset.

Software Reset Options

Two types of software resets can be applied to the device digital logic: soft reset and sticky reset. Soft reset and sticky reset create a reset pulse that is eight DAC_CLK cycles wide for the internal logic. These two reset commands are controlled by the REG_AFE032_CTL register. Sticky reset preserves all SPI register settings. In order to properly use the sticky reset, the values of all other control bits in the REG_AFE032_CTL register must be read and noted before asserting the sticky reset bit. Whatever is written to the REG_AFE032_CTL register is latched when performing a sticky reset. A soft reset, on the other hand, brings all device digital circuits to their default states.

After a soft reset or sticky reset is performed, a valid XCLK signal must be sent to the device for at least 65,536 cycles. The device must be reprogrammed because all control registers are now reset (with the exception of the REG_AFE032_CTL register bits in the case of a sticky reset).

AFE032 Interrupts

The device contains three maskable interrupt signals: IFLAG_INT, TFLAG_INT, and DIG_ERR_INT. These interrupt masks are set by default and can be changed by writing to the REG_FLAG_CTL register. The interrupt masks are used to prevent any or all interrupt signals from commanding the active-low, open-drain interrupt pin (INT). The REG_AFE_STATUS register contains the status of the three maskable interrupt signals; these signals operate as follows:

- IFLAG_INT: This interrupt is asserted when the PA goes to current limit mode for at least 16,384 DAC_CLK cycles. If the PA goes to current limit mode but then falls out of current limit mode before 16,384 DAC_CLK cycles have elapsed, then the IFLAG_INT is not set.
- TFLAG_INT: This interrupt is asserted when the PA goes to overtemperature mode.
- DIG_ERR_INT: This interrupt is a logical OR of all of individual interrupt vectors located in the REG_DIG_ERR register. See the Digital Interrupt Bits section and Table 26 for more detalis.

Note that reading the REG_AFE_STATUS register resets the IFLAG_INT and TFLAG_INT bits. Similarly, reading the REG_DIG_ERR register resets all of its bits. Note that the DIG_ERR_INT bit is not reset until the REG_DIG_ERR register is read.

Digital Interrupt Bits

The device can identify certain errors that may be caused because of improper programming or clocking. These errors are: AFIFO overflow, SPI write address fail, SPI illegal access, and SPI address error.

An AFIFO overflow error occurs if the ASYNCH FIFO used to convert DAC samples from the SPI to the DAC clock domain has overflowed. This error indicates that the external DSP is transmitting DAC samples at a rate (f_S) higher than the maximum capability of the device DSP path for the current configuration. Refer to the *SPI Clock To DAC Clock Synchronization* section for details on the proper selection of f_S and XCLK.

An SPI write address fail error occurs when a read-only register is attempted to be written to. An SPI illegal access error occurs when a reserved SPI register is attempted to be written to.

An SPI address error occurs when an SPI register is attempted to be accessed incorrectly. This error is caused by several reasons: if a reserved SPI register is attempted to be written to, if an SPI register is attempted to be accessed with an incorrect address (that is, an address that does not exist in Table 13), or if a read-only register is attempted to be written to.

Initialization Sequence

The following initialization sequence must be performed (in addition to the sequence described in the *Power-Up Sequence* section) to ensure the device is ready for communication to the power line each time power is applied to the device and each time after a soft reset is performed:

- Ensure the shutdown pin is low.
- Ensure a valid XCLK signal is present.
- Configure the device in SPI mode by taking the DAC pin low.
- Wait for at least 65,536 XCLK cycles.
- Enable the PA_NRF, TX_RX_NRF, and DAC_NRF blocks.
- Configure the two programmable clock dividers.
- Select the Tx filter band.
- Set the Enable assist bit (bit 7 in the REG_HPF/LPF_CFG register).
- Select which block in the digital path is used and which is bypassed.
- If block 4 is included, program the block 4 parameter of the DSP path.
- Set the Tx PGA, Rx PGA 1, and Rx PGA 2 gains.
- Enable the low-pass filter (LPF) and high-pass filter (HPF) according to the application requirements by writing to the REG_DAC/HPF/LPF/PA_CTL register. Make sure to enable the filter bias (bit 5 of the REG_DAC/HPF/LPF/PA_CTL register).
- Enable the DAC block by writing to register REG_DAC/HPF/LPF/PA_CTL (do not set the DAC pin high; just enable the DAC block to ensure the block is ready when the device is configured for transmission).
- Wait for two seconds to ensure all voltage references and signal path capacitors reach a steady state.

Power Amplifier Enable and Disable Sequences

Whether immediately after the initialization sequence or when transitioning from receiver mode to transmitter mode, one of the PA enable sequences described in this section must be used each time the device initiates a signal transmission on the power line via the power amplifier. The specific enable sequence used depends on whether the DAC block is enabled at least 300 µs prior to the start of the PA enable sequence or not.

PA Enable Sequence for a DAC Already Enabled Case

Use the following sequence if the DAC has been enabled for at least 300 µs.

- Simultaneously set the PA IQ current control bits (bits 6 and 7) and the PA current limit bits (bits 4 and 5) of the REG_PA_CURRENT_CFG register. The PA IQ current control bits must be set to '10' (that is, the 95 mA option). The PA current limit bit settings depend on the application.
- Enable the Filter bias enable bit (bit 5) of the REG_DAC/HPF/LPF/PA_CTL register.
- Write '1' to the TX enable bit (bit 4), and '0' to the RX enable bit (bit 3) of the REG_RX/TX_CTL register.
- Wait for 50 µs.
- Write B4 (hex) to the REG_DAC/HPF/LPF/PA_CTRL register. (This setting enables the PA internal sub-regulation circuitry, maintains the LPF and filter bias, and keeps the DAC enabled while leaving the HPF and PA output stage disabled.)
- Wait for 20 µs.
- Write BC (hex) to the REG_DAC/HPF/LPF/PA_CTRL register. (This setting enables the PA output stage while keeping the PA internal sub-regulation circuitry, LPF, filter bias, and DAC enabled. The HPF remains disabled.)
- Enable the ENPAIQN bit (bit 3) and the ENPAIQP bit (bit 2) of the REG_PA_CURRENT_CFG register.
- Enable the ENPCOMP bit (bit 7) and ENNCOMP bit (bit 6) of the REG_RX/TX_CTL register.
- Set the Tx PGA gain to the desired value.
- Wait for at least 20 DAC_CLK cycles.
- Configure the device in DAC mode by taking the DAC pin high.
- Write the desired samples to the DAC following the procedure outlined in the *DAC Mode* section.

PA Enable Sequence Starting from a DAC in Disabled State Case

Use the following sequence if the DAC is disabled or if it is enabled for less than 300 µs prior to the start of the PA enable sequence:

- Simultaneously set the PA IQ current control bits (bits 6 and 7) and PA current limit bits (bits 4 and 5) of the REG_PA_CURRENT_CFG register. The PA IQ current control bits must be set to '10' (that is, the 95 mA option). The PA current limit bit settings depend on the application.
- Enable the DAC by writing '1' to the DAC enable bit (bit 2) and the Filter bias enable bit (bit 5) of the REG_DAC/HPF/LPF/PA_CTL register.
- Write '1' to the TX enable bit (bit 4), and '0' to the RX enable bit (bit 3) of the REG_RX/TX_CTL register.
- Wait for 300 µs.
- Write B4 (hex) to the REG_DAC/HPF/LPF/PA_CTRL register. (This setting enables the PA internal sub-regulation circuitry, maintains the LPF and filter bias, and keeps the DAC enabled while leaving the HPF and PA output stage disabled.)
- Wait for 20 µs.
- Write BC (hex) to the REG_DAC/HPF/LPF/PA_CTRL register. (This setting enables the PA output stage while keeping the PA internal sub-regulation circuitry, LPF, filter bias, and DAC enabled. The HPF remains disabled.)
- Enable the ENPAIQN bit (bit 3) and the ENPAIQP bit (bit 2) of the REG_PA_CURRENT_CFG register.
- Enable the ENPCOMP bit (bit 7) and ENNCOMP bit (bit 6) of the REG_RX/TX_CTL register.
- Set the Tx PGA gain to the desired value.
- Wait for at least 20 DAC_CLK cycles.
- Configure the device in DAC mode by taking the DAC pin high.
- Write the desired samples to the DAC following the procedure outlined in the *DAC Mode* section.

PA Disable Sequence

Use the following sequence to disable the PA:

- Disable the PA output enable bit (bit 3) on the REG_DAC/HPF/LPF/PA_CTRL register.
- Disable the PA internal sub-regulation circuitry (bit 4) of the REG_DAC/HPF/LPF/PA_CTL register.
- Disable the ENPAIQN bit (bit 3) and the ENPAIQP bit (bit 2) of the REG_PA_CURRENT_CFG register.
- Disable the ENPCOMP bit (bit 7) and ENNCOMP bit (bit 6) of the REG_RX/TX_CTL register.
- Set the PA IQ current control bits (bits 6 and 7) of the REG_PA_CURRENT_CFG register to '00' (that is, the 55 mA option).

REGISTER MAP

The AFE032 data registers are listed in the memory map of Table 13. A description of each register is given in the *Register Description* section.

Table 13. Data Register Memory Map

<table>
<tr><th>REGISTER</th><th>ADDRESS (Hex)</th><th>DEFAULT VALUE (Hex)</th><th>BIT 7</th><th>BIT 6</th><th>BIT 5</th><th>BIT 4</th><th>BIT 3</th><th>BIT 2</th><th>BIT 1</th><th>BIT 0</th></tr>
<tr><td>REG_AFE032_CTL</td><td>00</td><td>00</td><td>Soft reset</td><td>Sticky reset</td><td>Reserved</td><td>Bypass Block 4</td><td>Bypass Block 3</td><td>Bypass Block 2</td><td>Bypass Block 1</td><td>DAC SPI select</td></tr>
<tr><td>REG_FLAG_CTL</td><td>01</td><td>E0</td><td>IFLAG mask</td><td>TFLAG mask</td><td>DIG_ERR mask</td><td colspan="5">Reserved</td></tr>
<tr><td>RESERVED</td><td>02</td><td>7F</td><td colspan="8">Reserved</td></tr>
<tr><td>REG_DAC/HPF/LPF/PA_CTL</td><td>03</td><td>00</td><td>LPF enable</td><td>HPF enable</td><td>Filter bias enable</td><td>PA enable</td><td>PA output enable</td><td>DAC enable</td><td>Reserved</td><td>Disable TLIM</td></tr>
<tr><td>REG_PA_CURRENT_CFG</td><td>04</td><td>00</td><td colspan="2">PA IQ current control</td><td colspan="2">PA current limit</td><td>ENPAIQN</td><td>ENPAIQP</td><td>ENPAICLN</td><td>ENPAICLP</td></tr>
<tr><td>REG_HPF/LPF_CFG</td><td>05</td><td>00</td><td>Enable Assist</td><td colspan="3">LPF band select</td><td>Reserved</td><td colspan="2">HPF band select</td><td>Reserved</td></tr>
<tr><td>REG_RX/TX_CTL</td><td>06</td><td>00</td><td>ENPCOMP</td><td>ENNCOMP</td><td>Reserved</td><td>Tx enable</td><td>Rx enable</td><td colspan="3">TX_PGA gain</td></tr>
<tr><td>REG_RX_PGA_CFG</td><td>07</td><td>00</td><td colspan="4">RX_PGA1 gain</td><td colspan="3">RX_PGA2 gain</td><td>Reserved</td></tr>
<tr><td>REG_VREF/ZEROX</td><td>08</td><td>00</td><td>Zero-cross1 detect enable</td><td>Zero-cross2 detect enable</td><td>Zero-cross3 detect enable</td><td>PA_NRF enable</td><td>TX_RX_NRF enable</td><td>DAC_NRF enable</td><td colspan="2">Reserved</td></tr>
<tr><td>RESERVED</td><td>09</td><td>18</td><td colspan="8">Reserved</td></tr>
<tr><td>REG_AFE_STATUS</td><td>0A</td><td>01</td><td>IFLAG_INT</td><td>TFLAG_INT</td><td>Reserved</td><td>DIG_ERR_INT</td><td colspan="4">Reserved</td></tr>
<tr><td>RESERVED</td><td>0B</td><td>00</td><td colspan="8">Reserved</td></tr>
<tr><td>RESERVED</td><td>0C</td><td>00</td><td colspan="8">Reserved</td></tr>
<tr><td>REG_DIG_ERROR</td><td>0D</td><td>00</td><td>Reserved</td><td>Reserved</td><td>AFIFO overflow</td><td>SPI write address fail</td><td>SPI illegal access</td><td>SPI address error</td><td colspan="2">Reserved</td></tr>
<tr><td>REG_ID</td><td>0E</td><td>00</td><td colspan="2">Die_ID</td><td colspan="3">Revision</td><td colspan="3">Reserved</td></tr>
<tr><td>REG_CLK_DIV</td><td>0F</td><td>03</td><td colspan="4">DAC clock POST_CLK_DIV</td><td colspan="4">DAC clock PRE_CLK_DIV</td></tr>
<tr><td>REG_OFFSET_0</td><td>10</td><td>F5</td><td colspan="8">Most significant byte of block 4 parameter</td></tr>
<tr><td>REG_OFFSET_1</td><td>11</td><td>C2</td><td colspan="8">Second to MSB of block 4 parameter</td></tr>
<tr><td>REG_OFFSET_2</td><td>12</td><td>8F</td><td colspan="8">Third to MSB of block 4 parameter</td></tr>
<tr><td>REG_OFFSET_3</td><td>13</td><td>5C</td><td colspan="8">Least significant byte of block 4 parameter</td></tr>
<tr><td>REG_CLIP_0</td><td>14</td><td>FF</td><td colspan="8">CLIP_MSB</td></tr>
<tr><td>REG_CLIP_1</td><td>15</td><td>E0</td><td colspan="3">CLIP_LSB</td><td colspan="5">Reserved</td></tr>
<tr><td>REG_CLIP_OFFSET_0</td><td>16</td><td>00</td><td colspan="8">CLIP_OFF_MSB</td></tr>
<tr><td>REG_CLIP_OFFSET_1</td><td>17</td><td>00</td><td colspan="3">CLIP_OFF_LSB</td><td colspan="5">Reserved</td></tr>
<tr><td>REG_AUX_CTL</td><td>18</td><td>26</td><td>Reserved</td><td>Reserved</td><td>DSP_CFG</td><td colspan="5">Reserved</td></tr>
<tr><td>RESERVED</td><td>19 to 23</td><td>00</td><td colspan="8">Reserved</td></tr>
<tr><td>REG_COEFF1_BLOCK_2_MS</td><td>24</td><td>B9</td><td colspan="8">Bits 11:4 of coefficient 1 for filter block 2</td></tr>
<tr><td>REG_COEFF1_BLOCK_2_LS</td><td>25</td><td>D0</td><td colspan="4">Bits 3:0 of coefficient 1 for filter block 2</td><td colspan="4">Reserved</td></tr>
<tr><td>REG_COEFF2_BLOCK_2_MS</td><td>26</td><td>E8</td><td colspan="8">Bits 11:4 of coefficient 2 for filter block 2</td></tr>
<tr><td>REG_COEFF2_BLOCK_2_LS</td><td>27</td><td>60</td><td colspan="4">Bits 3:0 of coefficient 2 for filter block 2</td><td colspan="4">Reserved</td></tr>
</table>

Table 13. Data Register Memory Map (continued)

REGISTER	ADDRESS (Hex)	DEFAULT VALUE (Hex)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
REG_COEFF3_BLOCK_2_MS	28	0F	Bits 11:4 of coefficient 3 for filter block 2							
REG_COEFF3_BLOCK_2_LS	29	00	Bits 3:0 of coefficient 3 for filter block 2				Reserved			
REG_COEFF4_BLOCK_2_MS	2A	1D	Bits 11:4 of coefficient 4 for filter block 2							
REG_COEFF4_BLOCK_2_LS	2B	C0	Bits 3:0 of coefficient 4 for filter block 2				Reserved			
REG_COEFF5_BLOCK_2_MS	2C	0F	Bits 11:4 of coefficient 5 for filter block 2							
REG_COEFF5_BLOCK_2_LS	2D	00	Bits 3:0 of coefficient 5 for filter block 2				Reserved			
REG_COEFF6_BLOCK_2_MS	2E	99	Bits 11:4 of coefficient 6 for filter block 2							
REG_COEFF6_BLOCK_2_LS	2F	40	Bits 3:0 of coefficient 6 for filter block 2				Reserved			
REG_COEFF7_BLOCK_2_MS	30	CA	Bits 11:4 of coefficient 7 for filter block 2							
REG_COEFF7_BLOCK_2_LS	31	10	Bits 3:0 of coefficient 7 for filter block 2				Reserved			
REG_COEFF8_BLOCK_2_MS	32	1F	Bits 11:4 of coefficient 8 for filter block 2							
REG_COEFF8_BLOCK_2_LS	33	20	Bits 3:0 of coefficient 8 for filter block 2				Reserved			
REG_COEFF9_BLOCK_2_MS	34	3B	Bits 11:4 of coefficient 9 for filter block 2							
REG_COEFF9_BLOCK_2_LS	35	10	Bits 3:0 of coefficient 9 for filter block 2				Reserved			
REG_COEFF10_BLOCK_2_MS	36	1F	Bits 11:4 of coefficient 10 for filter block 2							
REG_COEFF10_BLOCK_2_LS	37	20	Bits 3:0 of coefficient 10 for filter block 2				Reserved			
REG_COEFF11_BLOCK_2_MS	38	23	Bits 11:4 of coefficient 11 for filter block 2							
REG_COEFF11_BLOCK_2_LS	39	B0	Bits 3:0 of coefficient 11 for filter block 2				Reserved			
REG_COEFF12_BLOCK_2_MS	3A	44	Bits 11:4 of coefficient 12 for filter block 2							
REG_COEFF12_BLOCK_2_LS	3B	20	Bits 3:0 of coefficient 12 for filter block 2				Reserved			
REG_COEFF1_BLOCK_1_MS	3C	B9	Bits 11:4 of coefficient 1 for filter block 1							
REG_COEFF1_BLOCK_1_LS	3D	D0	Bits 3:0 of coefficient 1 for filter block 1				Reserved			
REG_COEFF2_BLOCK_1_MS	3E	E8	Bits 11:4 of coefficient 2 for filter block 1							
REG_COEFF2_BLOCK_1_LS	3F	60	Bits 3:0 of coefficient 2 for filter block 1				Reserved			
REG_COEFF3_BLOCK_1_MS	40	0F	Bits 11:4 of coefficient 3 for filter block 1							
REG_COEFF3_BLOCK_1_LS	41	00	Bits 3:0 of coefficient 3 for filter block 1				Reserved			
REG_COEFF4_BLOCK_1_MS	42	1D	Bits 11:4 of coefficient 4 for filter block 1							
REG_COEFF4_BLOCK_1_LS	43	C0	Bits 3:0 of coefficient 4 for filter block 1				Reserved			
REG_COEFF5_BLOCK_1_MS	44	0F	Bits 11:4 of coefficient 5 for filter block 1							
REG_COEFF5_BLOCK_1_LS	45	00	Bits 3:0 of coefficient 5 for filter block 1				Reserved			
REG_COEFF6_BLOCK_1_MS	46	23	Bits 11:4 of coefficient 6 for filter block 1							
REG_COEFF6_BLOCK_1_LS	47	B0	Bits 3:0 of coefficient 6 for filter block 1				Reserved			
REG_COEFF7_BLOCK_1_MS	48	44	Bits 11:4 of coefficient 7 for filter block 1							
REG_COEFF7_BLOCK_1_LS	49	20	Bits 3:0 of coefficient 7 for filter block 1				Reserved			
REG_DAC_SAMPLE_MS	4A	00	Bits 11:4 of DAC sample fed from DSP path into DAC							
REG_DAC_SAMPLE_LS	4B	00	Bits 3:0 of DAC sample fed from DSP path into DAC				Reserved			

Register Description

Table 14. REG_AFE032_CTL Register (Address = 00h)

7	6	5	4	3	2	1	0
Soft reset	Sticky reset	Reserved	Bypass Block 4	Bypass Block 3	Bypass Block 2	Bypass Block 1	DAC SPI select
R0/W	R0/W	R	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = read and write; R0/W = read '0' and write (these bits always reset to '0' after being written); R = read-only.

Bit 7 **Soft reset**

This bit creates a reset pulse to all AFE digital circuits and control registers. This bit is self resetting.

0 = Normal operation (default)
1 = Reset

Bit 6 **Sticky reset**

This bit resets all AFE digital circuits except the SPI registers. The SPI registers maintain all currently programmed values. This bit is self resetting.

0 = Normal operation (default)
1 = Reset

Bit 5 **Reserved**

This bit is reserved.
Default = 0.

Bit 4 **Bypass Block 4**

This bit determines if block 4 is included in the signal path.

0 = Include block 4 (default)
1 = Bypass block 4

Bit 3 **Bypass Block 3**

This bit determines if block 3 is included in the signal path.

0 = Include block 3 (default)
1 = Bypass block 3

Bit 2 **Bypass Block 2**

This bit determines if block 2 is included in the signal path.

0 = Include block 2 (default)
1 = Bypass block 2

Bit 1 **Bypass Block 1**

This bit determines if block 1 is included in the signal path.

0 = Include block 1 (default)
1 = Bypass block 1

Bit 0 **DAC SPI select**

This bit sets the 12-bit DAC sample in either a 16-bit SCLK envelope or a 12-bit SCLK envelope.

0 = 12-bit DAC burst (default)
1 = 16-bit DAC burst

Table 15. REG_FLAG_CTL Register (Address = 01h)

7	6	5	4	3	2	1	0
IFLAG mask	TFLAG mask	DIG_ERR mask	Reserved				
R/W	R/W	R/W	R				

LEGEND: R/W = read and write; R = read-only.

Bit 7 **IFLAG mask**

Software asserts this bit to prevent the current-limit interrupt from commanding the INT external pin. The current limit event still asserts the IFLAG_INT bit on the REG_AFE_STATUS register.

0 = Do not mask
1 = Mask IFLAG_INT (default)

Bit 6 **TFLAG mask**

Software asserts this bit to prevent the overtemperature interrupt from commanding the INT external pin. The overtemperature event still asserts the TFLAG_INT bit on the REG_AFE_STATUS register.

0 = Do not mask
1 = Mask TFLAG_INT (default)

Bit 5 **DIG_ERR mask**

Software asserts this bit to prevent the digital error status bits from commanding the INT external pin. Any digital errors can still be read in the REG_DIG_ERROR register.

0 = Do not mask
1 = Mask digital errors (default)

Bits[4:0] **Reserved**

These bits are reserved.
Default = 0.

Table 16. RESERVED Register (Address = 02h)

7	6	5	4	3	2	1	0
Reserved							
R							

LEGEND: R = read-only.

This register is reserved. Default = 7Fh

Table 17. REG_DAC/HPF/LPF/PA_CTRL Register (Address = 03h)

7	6	5	4	3	2	1	0
LPF enable	HPF enable	Filter bias enable	PA enable	PA output enable	DAC enable	Reserved	Disable TLIM
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = read and write.

Bit 7 **LPF enable**

This bit enables and disables the programmable analog low-pass filter (LPF).

0 = LPF disabled (default)
1 = LPF enabled

Bit 6 **HPF enable**

This bit enables and disables the programmable analog high-pass filter (HPF).

0 = HPF disabled (default)
1 = HPF enabled

Bit 5 **Filter bias enable**

This bit enables and disables the programmable LPF and HPF. For normal Rx or Tx operation, this bit remains enabled. For power-down operation, this bit is disabled by placing the analog filters in low-power mode with high output impedance.

0 = Disabled (default)
1 = Enable filter bias

Bit 4 **PA enable**

This bit enables and disables the internal sub-regulation circuitry of the power amplifier.

0 = Disabled (default)
1 = PA enabled

Bit 3 **PA output enable**

This bit enables the PA output stage. When enabled, the PA output stage functions normally with a low output impedance capable of driving heavy loads. When disabled, the PA output stage is placed in a high-impedance state.

0 = Disabled (default)
1 = PA output enabled

Bit 2 **DAC enable**

This bit enables and disables the DAC.

0 = DAC disabled (default)
1 = DAC enabled

Bit 1 **Reserved**

This bit is reserved.
Default = 0

Bit 0 **Disable TLIM**

This bit enables and disables the PA thermal shutdown circuitry. Warning: keeping the PA thermal shutdown circuitry enabled to prevent potential permanent damage to the device is strongly recommended. See the *Thermal Overload* section for more details.

0 = PA TLIM enabled (default)
1 = PA TLIM disabled

Table 18. REG_PA_CURRENT_CFG Register (Address = 04h)

7	6	5	4	3	2	1	0
PA IQ current control		PA current limit		ENPAIQN	ENPAIQP	ENPAICLN	ENPAICLP
R/W		R/W		R/W	R/W	R/W	R/W

LEGEND: R/W = read and write.

Bits[7:6] **PA IQ current control**

These bits control the PA programmable quiescent current.

00 = > 55 mA, typ (default)
01 = > 80 mA, typ
10 = > 95 mA, typ
11 = > 25 mA, typ

Bits[5:4] **PA current limit**

These bits control the PA programmable current limit.

00 = > 1.25 A, typ (default)
01 = > 1.8 A, typ
10 = > 2.5 A, typ
11 = > 3.0 A, typ

Bit 3 **ENPAIQN**

This bit enables and disables the PA quiescent current negative bias circuitry.

0 = Disabled (default)
1 = Enabled

Bit 2 **ENPAIQP**

This bit enables and disables the PA quiescent current positive bias circuitry.

0 = Disabled (default)
1 = Enabled

Bit 1 **ENPAICLN**

This bit enables and disables the PA negative current limit circuitry.

0 = The PA negative current limit circuitry is enabled and protects the device (default)
1 = The PA negative current limit circuitry is disabled and the device is at risk of permanent damage if a current overload event occurs

Bit 0 **ENPAICLP**

This bit enables and disables the PA positive current limit circuitry.

0 = The PA positive current limit circuitry is enabled and protects the device (default)
1 = The PA positive current limit circuitry is disabled and the device is at risk of permanent damage if a current overload event occurs

Table 19. REG_HPF/LPF_CFG Register (Address = 05h)

7	6	5	4	3	2	1	0
Enable assist	LPF band select			Reserved	HPF band select		Reserved
R/W	R/W			R/W	R/W		R

LEGEND: R/W = read and write; R = read only.

Bit 7 **Enable assist**

This bit must be asserted as part of the analog signal chain (Tx and Rx PGAs and filters) enabling process.

0 = Enable assist circuitry is not engaged (default)

1 = Enable assist circuitry is engaged (recommended for best performance)

Bits[6:4] **LPF band select**

This bit selects the programmable analog LPF cutoff frequency.

000 = 95 kHz (default)
001 = 150 kHz
010 = 420 kHz
011 = 490 kHz

Bit 3 **Reserved**

This bit is reserved.
Default = 0

Bits[2:1] **HPF band select**

This bit selects the programmable analog HPF cutoff frequency.

00 = 35 kHz (default)
01 = 150 kHz

Bit 0 **Reserved**

This bit is reserved.
Default = 0

Table 20. REG_RX/TX_CTL Register (Address = 06h)

7	6	5	4	3	2	1	0
ENPCOMP	ENNCOMP	Reserved	TX enable	RX enable	TX_PGA gain		
R/W	R/W	R/W	R/W	R/W	R/W		

LEGEND: R/W = read and write.

Bit 7 **ENPCOMP**

This bit enables the PA positive start control.

0 = Disabled (default)
1 = Enabled

Bit 6 **ENNCOMP**

This bit enables the PA negative start control.

0 = Disabled (default)
1 = Enabled

Bit 5 **Reserved**

This bit is reserved.
Default = 0

Bit 4 **TX enable**

This bit enables and disables TX_PGA and configures the programmable filter for either Tx or Rx mode.

0 = Tx path disabled (default)
1 = Tx path enabled

Bit 3 **RX enable**

This bit enables and disables RX_PGA1 and RX_PGA2. This bit can either be left enabled or disabled during Tx mode.

0 = Rx disabled (default)
1 = Rx enabled

Bits[2:0] **TX_PGA gain**

These bits select the TX_PGA gain.

000 = 1.15 (default)
001 = 2.3
010 = 3.25
011 = 4.6

Table 21. REG_RXPGA_CFG Register (Address = 07h)

7	6	5	4	3	2	1	0
RX_PGA1 gain				RX_PGA2 gain			Reserved
R/W				R/W			R/W

LEGEND: R/W = read and write.

Bits[7:4] **RX_PGA1 gain**

These bits select the RX_PGA1 gain.

0000 = 0.125 (default)
0001 = 0.25
0010 = 0.5
0011 = 1
0100 = 2
0101 = 4
0110 = 8
0111 = 16
1000 = 32

Bits[3:1] **RX_PGA2 gain**

These bits select the RX_PGA2 gain.

000 = 1 (default)
001 = 4
010 = 16

Bit 0 **Reserved**

This bit is reserved.
Default = 0

Table 22. REG_VREF/ZEROX Register (Address = 08h)

7	6	5	4	3	2	1	0
Zero-cross1 detect enable	Zero-cross2 detect enable	Zero-cross3 detect enable	PA_NRF enable	TX_RX_NRF enable	DAC_NRF enable	Reserved	
R/W	R/W	R/W	R/W	R/W	R/W	R	

LEGEND: R/W = read and write; R = read-only.

Bit 7 **Zero-cross1 detect enable**

This bit enables and disables the zero-crossing 1 detector.

0 = Disabled (default)
1 = Enabled

Bit 6 **Zero-cross2 detect enable**

This bit enables and disables the zero-crossing 2 detector.

0 = Disabled (default)
1 = Enabled

Bit 5 **Zero-cross3 detect enable**

This bit enables and disables the zero-crossing 3 detector.

0 = Disabled (default)
1 = Enabled

Bit 4 **PA_NRF enable**

This bit enables and disables the PA noise-reducing filter (NRF) and internal reference bias generator. For normal operation, this bit is enabled. This bit is disabled during operational conditions requiring maximum power savings. The device cannot transmit when this bit is disabled.

0 = Disabled (default)
1 = Enabled

Bit 3 **TX_RX_NRF enable**

This bit enables and disables the Tx and Rx NRF and internal reference bias generator. For normal operation, this bit is enabled. This bit is disabled during operational conditions requiring maximum power savings. The device cannot transmit or receive when this bit is disabled.

0 = Disabled (default)
1 = Enabled

Bit 2 **DAC_NRF enable**

This bit enables and disables the DAC NRF and internal reference bias generator. For normal operation, this bit is enabled. This bit is disabled during operational conditions requiring maximum power savings. The device cannot transmit when this bit is disabled.

0 = Disabled (default)
1 = Enabled

Bits[1:0] **Reserved**

These bits are reserved.
Default = 0

Table 23. RESERVED Register (Address = 09h)

7	6	5	4	3	2	1	0
Reserved							
R							

LEGEND: R = read-only.

This register is reserved. Default = 18h

Table 24. REG_AFE_STATUS Register (Address = 0Ah)

7	6	5	4	3	2	1	0
IFLAG_INT	TFLAG_INT	Reserved	DIG_ERR_INT	Reserved			
R0	R0	R0	R	R			

LEGEND: R/W = read and write; R = read-only; R0 = read '0' (these bits reset to '0' after being read).

Bit 7 **IFLAG_INT**

This bit is set when the PA enters the current limit state for at least 16,384 DAC_CLK cycles. This interrupt is cleared after being read.

0 = PA current limit not detected (default)
1 = PA current limit detected

Bit 6 **TFLAG_INT**

This bit is set when the PA enters the thermal limit state. This interrupt is cleared after being read.

0 = PA thermal limit not detected (default)
1 = PA thermal limit detected

Bit 5 **Reserved**

This bit is reserved.
Default = 0

Bit 4 **DIG_ERR_INT**

This bit is set when a digital error is detected. The REG_DIG_ERROR register must be read in order to clear this interrupt.

0 = Digital errors not detected (default)
1 = Digital errors detected

Bits[3:0] **Reserved**

These bits are reserved.
Default = not applicable

Table 25. RESERVED Registers (Address = 0Bh to 0Ch)

7	6	5	4	3	2	1	0
Reserved							
R							

LEGEND: R = read-only.

These registers are reserved.

Table 26. REG_DIG_ERROR Register (Address = 0Dh)

7	6	5	4	3	2	1	0
Reserved	Reserved	AFIFO overflow	SPI write address fail	SPI illegal access	SPI address error	Reserved	
R0	R0	R0	R0	R0	R0	R	

LEGEND: R = read-only; R0 = read '0' (these bits reset to '0' after being read).

This register is comprised of digital logic error detection bits. All bits are reset to '0' when read.

Bits[7:6] **Reserved**

Reserved
Default = 0

Bit 5 **AFIFO overflow**

SPI and DAC ASYNCH FIFO overflow.

0 = Normal operation (default)
1 = Error detected

Bit 4 **SPI write address fail**

An error indicates that a read-only register was attempted to be written to.

0 = Normal operation (default)
1 = Error detected

Bit 3 **SPI illegal access**

An error indicates that a register reserved for factory testing and trimming was attempted to be written to.

0 = Normal operation (default)
1 = Error detected

Bit 2 **SPI address error**

An error indicates that either a nonexistent register, a reserved register, or a read-only register was attempted to be written to.

0 = Normal operation (default)
1 = Error detected

Bits 1:0 **Reserved**

These bits are reserved.
Default = 0

Table 27. REG_ID Register (Address = 0Eh)

7	6	5	4	3	2	1	0
Die_ID		Revision			Reserved		
R		R			R		

LEGEND: R = read-only.

Bits[7:6] **Die_ID**

These bits are the die identification.
Default = 0

Bits[5:3] **Revision**

These bits are the revision indicator.
Default = 0

Bits[2:0] **Reserved**

These bits are reserved.
Default = 0

Table 28. REG_CLK_DIV Register (Address = 0Fh)

7	6	5	4	3	2	1	0
DAC clock POST_CLK_DIV				DAC clock PRE_CLK_DIV			
R/W				R/W			

LEGEND: R/W = read and write.

Bits[7:4] **DAC clock POST_CLK_DIV**

Internal DAC clock divider offset.

These bits control the value of the second clock divider. DAC_CLK is related to XCLK by: XCLK = (PRE_CLK_DIV + 1) × (POST_CLK_DEV + 1) x DAC_CLK.
Default = 0

Bits[3:0] **DAC clock PRE_CLK_DIV**

Internal DAC clock divider offset.

These bits control the value of the first clock divider. DAC_CLK is related to XCLK by: XCLK = (PRE_CLK_DIV + 1) × (POST_CLK_DEV + 1) x DAC_CLK.
Default = 3h

Table 29. REG_OFFSET_0 Register (Address = 10h)

7	6	5	4	3	2	1	0
Most significant byte of block 4 parameter							
R/W							

LEGEND: R/W = read and write.

Bits[7:0] **Most significant byte of block 4 parameter**

These bits are the MSB of the 32-bit parameter for block 4 of the DSP path.
Default = F5h

Table 30. REG_OFFSET_1 Register (Address = 11h)

7	6	5	4	3	2	1	0
Second to MSB of block 4 parameter							
R/W							

LEGEND: R/W = read and write.

Bits[7:0] **Second to MSB of block 4 parameter**

These bits are second in line to the MSB of the block 4 parameter.
Default = C2h

Table 31. REG_OFFSET_2 Register (Address = 12h)

7	6	5	4	3	2	1	0
Third to MSB of block 4 parameter							
R/W							

LEGEND: R/W = read and write.

Bits[7:0] **Third to MSB of block 4 parameter**

These bits are third in line to the MSB of the block 4 parameter.
Default = 8Fh

Table 32. REG_OFFSET_3 Register (Address = 13h)

7	6	5	4	3	2	1	0
Least significant byte of block 4 parameter							
R/W							

LEGEND: R/W = read and write.

Bits[7:0] **Least significant byte of block 4 parameter**

These bits are the LSB of the block 4 parameter.
Default = 5Ch

Table 33. REG_CLIP_0 Register (Address = 14h)

7	6	5	4	3	2	1	0
CLIP_MSB							
R/W							

LEGEND: R/W = read and write.

Bits[7:0] **CLIP_MSB**

These bits are the MSB of the 11-bit clip value. Input samples to the DAC are clipped by this value.

These bits control DAC_CLIP[10:3].
Default = FFh

Table 34. REG_CLIP_1 Register (Address = 15h)

7	6	5	4	3	2	1	0
CLIP_LSB			Reserved				
R/W			R0				

LEGEND: R/W = read and write; R0 = read '0' (these bits reset to '0' after being read).

Bits[7:5] **CLIP_LSB**

These bits are the LSB of the 11-bit clip value. Input samples to the DAC are clipped by this value.

These bits control DAC_CLIP[2:0].
Default = 07h

Bits[4:0] **Reserved**

These bits are reserved.
Default = 0

Table 35. REG_CLIP_OFFSET_0 Register (Address = 16h)

7	6	5	4	3	2	1	0
CLIP_OFF_MSB							
R/W							

LEGEND: R/W = read and write.

Bits[7:0] **CLIP_OFF_MSB**

These bits are the MSB of the 11-bit clip offset value. Clipped DAC samples have this offset subtracted from the clipped value.

These bits control DAC_CLIP_OFF[10:3].
Default = 0

Table 36. REG_CLIP_OFFSET_1 Register (Address = 17h)

7	6	5	4	3	2	1	0
CLIP_OFF_LSB			Reserved				
R/W			R				

LEGEND: R/W = read and write; R = read-only.

Bits[7:5] **CLIP_OFF_LSB**

These bits are the LSB of the 11-bit clip offset value. Clipped DAC Samples have this offset subtracted from the clipped value.

These bits control DAC_CLIP_OFF[2:0].
Default = 0

Bits[4:0] **Reserved**

These bits are reserved.
Default = 0

Table 37. REG_AUX_CTL Register (Address = 18h)

7	6	5	4	3	2	1	0
Reserved	Reserved	DSP_CFG	Reserved				Reserved
R/W	R/W	R/W	R/W				R

LEGEND: R/W = read and write; R = read-only.

Bits[7:6] **Reserved**

This bits are reserved.
Default = 0

Bit 5 **DSP_CFG**

This bit allows the state of the DSP blocks to be retained or to be forced to their reset values during SPI mode.

0 = Hold the state of the DSP path blocks when the device is in SPI mode (default)
1 = Reset the state of the DSP path when the device is in DAC mode

Bits[4:1] **Reserved**

These bits are reserved.
Default = 3h

Bit 0 **Reserved**

This bit is reserved.
Default = 0

Table 38. RESERVED Registers (Address = 19h to 23h)

7	6	5	4	3	2	1	0
Reserved							
R							

LEGEND: R = read-only.

These registers are reserved.

Table 39. REG_COEFF1_BLOCK_2_MS Register (Address = 24h)

7	6	5	4	3	2	1	0
Bits 11:4 of coefficient 1 for filter block 2							
R/W							

LEGEND: R/W = read and write.

Bits [7:0] **Bits 11:4 of coefficient 1 for filter block 2**

These bits contain the eight most significant bits of coefficient 1 for filter block 2.

Default = B9h

Table 40. REG_COEFF1_BLOCK_2_LS Register (Address = 25h)

7	6	5	4	3	2	1	0
Bits 3:0 of coefficient 1 for filter block 2				Reserved			
R/W				R			

LEGEND: R/W = read and write; R = read-only.

Bits [7:4] **Bits 3:0 of coefficient 1 for filter block 2**

These bits contain the four least significant bits of coefficient 1 for filter block 2.

Default = Dh

Bits [3:0] **Reserved**

These bits are reserved.
Default = not applicable

Table 41. REG_COEFF2_BLOCK_2_MS Register (Address = 26h)

7	6	5	4	3	2	1	0
Bits 11:4 of coefficient 2 for filter block 2							
R/W							

LEGEND: R/W = read and write.

Bits [7:0] **Bits 11:4 of coefficient 2 for filter block 2**

These bits contain the eight most significant bits of coefficient 2 for filter block 2.

Default = E8h

Table 42. REG_COEFF2_BLOCK_2_LS Register (Address = 27h)

7	6	5	4	3	2	1	0
Bits 3:0 of coefficient 2 for filter block 2				Reserved			
R/W				R			

LEGEND: R/W = read and write; R = read-only.

Bits [7:4] **Bits 3:0 of coefficient 2 for filter block 2**

These bits contain the four least significant bits of coefficient 2 for filter block 2.

Default = 6h

Bits [3:0] **Reserved**

These bits are reserved.
Default = not applicable

Table 43. REG_COEFF3_BLOCK_2_MS Register (Address = 28h)

7	6	5	4	3	2	1	0
Bits 11:4 of coefficient 3 for filter block 2							
R/W							

LEGEND: R/W = read and write.

Bits [7:0] **Bits 11:4 of coefficient 3 for filter block 2**

These bits contain the eight most significant bits of coefficient 3 for filter block 2.

Default = 0Fh

Table 44. REG_COEFF3_BLOCK_2_LS Register (Address = 29h)

7	6	5	4	3	2	1	0
Bits 3:0 of coefficient 3 for filter block 2				Reserved			
R/W				R			

LEGEND: R/W = read and write; R = read-only.

Bits [7:4] **Bits 3:0 of coefficient 3 for filter block 2**

These bits contain the four least significant bits of coefficient 3 for filter block 2.

Default = 0h

Bits [3:0] **Reserved**

These bits are reserved.
Default = not applicable

Table 45. REG_COEFF4_BLOCK_2_MS Register (Address = 2Ah)

7	6	5	4	3	2	1	0
Bits 11:4 of coefficient 4 for filter block 2							
R/W							

LEGEND: R/W = read and write.

Bits [7:0] **Bits 11:4 of coefficient 4 for filter block 2**

These bits contain the eight most significant bits of coefficient 4 for filter block 2.

Default = 1Dh

Table 46. REG_COEFF4_BLOCK_2_LS Register (Address = 2Bh)

7	6	5	4	3	2	1	0
Bits 3:0 of coefficient 4 for filter block 2				Reserved			
R/W				R			

LEGEND: R/W = read and write; R = read-only.

Bits [7:4] **Bits 3:0 of coefficient 4 for filter block 2**

These bits contain the four least significant bits of coefficient 4 for filter block 2.

Default = Ch

Bits [3:0] **Reserved**

These bits are reserved.
Default = not applicable

Table 47. REG_COEFF5_BLOCK_2_MS Register (Address = 2Ch)

7	6	5	4	3	2	1	0
Bits 11:4 of coefficient 5 for filter block 2							
R/W							

LEGEND: R/W = read and write.

Bits [7:0] **Bits 11:4 of coefficient 5 for filter block 2**

These bits contain the eight most significant bits of coefficient 5 for filter block 2.

Default = 0Fh

Table 48. REG_COEFF5_BLOCK_2_LS Register (Address = 2Dh)

7	6	5	4	3	2	1	0
Bits 3:0 of coefficient 5 for filter block 2				Reserved			
R/W				R			

LEGEND: R/W = read and write; R = read-only.

Bits [7:4] **Bits 3:0 of coefficient 5 for filter block 2**

These bits contain the four least significant bits of coefficient 5 for filter block 2.

Default = 0h

Bits [3:0] **Reserved**

These bits are reserved.
Default = not applicable

Table 49. REG_COEFF6_BLOCK_2_MS Register (Address = 2Eh)

7	6	5	4	3	2	1	0
Bits 11:4 of coefficient 6 for filter block 2							
R/W							

LEGEND: R/W = read and write.

Bits [7:0] **Bits 11:4 of coefficient 6 for filter block 2**

These bits contain the eight most significant bits of coefficient 6 for filter block 2.

Default = 99h

Table 50. REG_COEFF6_BLOCK_2_LS Register (Address = 2Fh)

7	6	5	4	3	2	1	0
Bits 3:0 of coefficient 6 for filter block 2				Reserved			
R/W				R			

LEGEND: R/W = read and write; R = read-only.

Bits [7:4] **Bits 3:0 of coefficient 6 for filter block 2**

These bits contain the four least significant bits of coefficient 6 for filter block 2.

Default = 4h

Bits [3:0] **Reserved**

These bits are reserved.
Default = not applicable

Table 51. REG_COEFF7_BLOCK_2_MS Register (Address = 30h)

7	6	5	4	3	2	1	0
Bits 11:4 of coefficient 7 for filter block 2							
R/W							

LEGEND: R/W = read and write.

Bits [7:0] **Bits 11:4 of coefficient 7 for filter block 2**

These bits contain the eight most significant bits of coefficient 7 for filter block 2.

Default = CAh

Table 52. REG_COEFF7_BLOCK_2_LS Register (Address = 31h)

7	6	5	4	3	2	1	0
Bits 3:0 of coefficient 7 for filter block 2				Reserved			
R/W				R			

LEGEND: R/W = read and write; R = read-only.

Bits [7:4] **Bits 3:0 of coefficient 7 for filter block 2**

These bits contain the four least significant bits of coefficient 7 for filter block 2.

Default = 1h

Bits [3:0] **Reserved**

These bits are reserved.
Default = not applicable

Table 53. REG_COEFF8_BLOCK_2_MS Register (Address = 32h)

7	6	5	4	3	2	1	0
Bits 11:4 of coefficient 8 for filter block 2							
R/W							

LEGEND: R/W = read and write.

Bits [7:0] **Bits 11:4 of coefficient 8 for filter block 2**

These bits contain the eight most significant bits of coefficient 8 for filter block 2.

Default = 1Fh

Table 54. REG_COEFF8_BLOCK_2_LS Register (Address = 33h)

7	6	5	4	3	2	1	0
Bits 3:0 of coefficient 8 for filter block 2				Reserved			
R/W				R			

LEGEND: R/W = read and write; R = read-only.

Bits [7:4] **Bits 3:0 of coefficient 8 for filter block 2**

These bits contain the four least significant bits of coefficient 8 for filter block 2.

Default = 2h

Bits [3:0] **Reserved**

These bits are reserved.
Default = not applicable

Table 55. REG_COEFF9_BLOCK_2_MS Register (Address = 34h)

7	6	5	4	3	2	1	0
Bits 11:4 of coefficient 9 for filter block 2							
R/W							

LEGEND: R/W = read and write.

Bits [7:0] **Bits 11:4 of coefficient 9 for filter block 2**

These bits contain the eight most significant bits of coefficient 9 for filter block 2.

Default = 3Bh

Table 56. REG_COEFF9_BLOCK_2_LS Register (Address = 35h)

7	6	5	4	3	2	1	0
Bits 3:0 of coefficient 9 for filter block 2				Reserved			
R/W				R			

LEGEND: R/W = read and write; R = read-only.

Bits [7:4] **Bits 3:0 of coefficient 9 for filter block 2**

These bits contain the four least significant bits of coefficient 9 for filter block 2.

Default = 1h

Bits [3:0] **Reserved**

These bits are reserved.
Default = not applicable

Table 57. REG_COEFF10_BLOCK_2_MS Register (Address = 36h)

7	6	5	4	3	2	1	0
Bits 11:4 of coefficient 10 for filter block 2							
R/W							

LEGEND: R/W = read and write.

Bits [7:0] **Bits 11:4 of coefficient 10 for filter block 2**

These bits contain the eight most significant bits of coefficient 10 for filter block 2.

Default = 1Fh

Table 58. REG_COEFF10_BLOCK_2_LS Register (Address = 337h)

7	6	5	4	3	2	1	0
Bits 3:0 of coefficient 10 for filter block 2				Reserved			
R/W				R			

LEGEND: R/W = read and write; R = read-only.

Bits [7:4] **Bits 3:0 of coefficient 10 for filter block 2**

These bits contain the four least significant bits of coefficient 10 for filter block 2.

Default = 2h

Bits [3:0] **Reserved**

These bits are reserved.
Default = not applicable

Table 59. REG_COEFF11_BLOCK_2_MS Register (Address = 38h)

7	6	5	4	3	2	1	0
Bits 11:4 of coefficient 11 for filter block 2							
R/W							

LEGEND: R/W = read and write.

Bits [7:0] **Bits 11:4 of coefficient 11 for filter block 2**

These bits contain the eight most significant bits of coefficient 11 for filter block 2.

Default = 23h

Table 60. REG_COEFF11_BLOCK_2_LS Register (Address = 39h)

7	6	5	4	3	2	1	0
Bits 3:0 of coefficient 11 for filter block 2				Reserved			
R/W				R			

LEGEND: R/W = read and write; R = read-only.

Bits [7:4] **Bits 3:0 of coefficient 11 for filter block 2**

These bits contain the four least significant bits of coefficient 11 for filter block 2.

Default = Bh

Bits [3:0] **Reserved**

These bits are reserved.
Default = not applicable

Table 61. REG_COEFF12_BLOCK_2_MS Register (Address = 3Ah)

7	6	5	4	3	2	1	0
Bits 11:4 of coefficient12 for filter block 2							
R/W							

LEGEND: R/W = read and write.

Bits [7:0] **Bits 11:4 of coefficient 12 for filter block 2**

These bits contain the eight most significant bits of coefficient 12 for filter block 2.

Default = 44h

Table 62. REG_COEFF12_BLOCK_2_LS Register (Address = 3Bh)

7	6	5	4	3	2	1	0
Bits 3:0 of coefficient 12 for filter block 2				Reserved			
R/W				R			

LEGEND: R/W = read and write; R = read-only.

Bits [7:4] **Bits 3:0 of coefficient 12 for filter block 2**

These bits contain the four least significant bits of coefficient 12 for filter block 2.

Default = 2h

Bits [3:0] **Reserved**

These bits are reserved.
Default = not applicable

Table 63. REG_COEFF1_BLOCK_1_MS Register (Address = 3Ch)

7	6	5	4	3	2	1	0
Bits 11:4 of coefficient 1 for filter block 1							
R/W							

LEGEND: R/W = read and write.

Bits [7:0] **Bits 11:4 of coefficient 1 for filter block 1**

These bits contain the eight most significant bits of coefficient 1 for filter block 1.

Default = B9h

Table 64. REG_COEFF1_BLOCK_1_LS Register (Address = 3Dh)

7	6	5	4	3	2	1	0
Bits 3:0 of coefficient 1 for filter block 1				Reserved			
R/W				R			

LEGEND: R/W = read and write; R = read-only.

Bits [7:4] **Bits 3:0 of coefficient 1 for filter block 1**

These bits contain the four least significant bits of coefficient 1 for filter block 1.

Default = Dh

Bits [3:0] **Reserved**

These bits are reserved.
Default = not applicable

Table 65. REG_COEFF2_BLOCK_1_MS Register (Address = 3Eh)

7	6	5	4	3	2	1	0
Bits 11:4 of coefficient 2 for filter block 1							
R/W							

LEGEND: R/W = read and write.

Bits [7:0] **Bits 11:4 of coefficient 2 for filter block 1**

These bits contain the eight most significant bits of coefficient 2 for filter block 1.

Default = E8h

Table 66. REG_COEFF2_BLOCK_1_LS Register (Address = 3Fh)

7	6	5	4	3	2	1	0
Bits 3:0 of coefficient 2 for filter block 1				Reserved			
R/W				R			

LEGEND: R/W = read and write; R = read-only.

Bits [7:4] **Bits 3:0 of coefficient 2 for filter block 1**

These bits contain the four least significant bits of coefficient 2 for filter block 1.

Default = 6h

Bits [3:0] **Reserved**

These bits are reserved.
Default = not applicable

Table 67. REG_COEFF3_BLOCK_1_MS Register (Address = 40h)

7	6	5	4	3	2	1	0
Bits 11:4 of coefficient 3 for filter block 1							
R/W							

LEGEND: R/W = read and write.

Bits [7:0] **Bits 11:4 of coefficient 3 for filter block 1**

These bits contain the eight most significant bits of coefficient 3 for filter block 1.

Default = 0Fh

Table 68. REG_COEFF3_BLOCK_1_LS Register (Address = 41h)

7	6	5	4	3	2	1	0
Bits 3:0 of coefficient 3 for filter block 1				Reserved			
R/W				R			

LEGEND: R/W = read and write; R = read-only.

Bits [7:4] **Bits 3:0 of coefficient 3 for filter block 1**

These bits contain the four least significant bits of coefficient 3 for filter block 1.

Default = 0h

Bits [3:0] **Reserved**

These bits are reserved.
Default = not applicable

Table 69. REG_COEFF4_BLOCK_1_MS Register (Address = 42h)

7	6	5	4	3	2	1	0
Bits 11:4 of coefficient 4 for filter block 1							
R/W							

LEGEND: R/W = read and write.

Bits [7:0] **Bits 11:4 of coefficient 4 for filter block 1**

These bits contain the eight most significant bits of coefficient 4 for filter block 1.

Default = 1Dh

Table 70. REG_COEFF4_BLOCK_1_LS Register (Address = 43h)

7	6	5	4	3	2	1	0
Bits 3:0 of coefficient 4 for filter block 1				Reserved			
R/W				R			

LEGEND: R/W = read and write; R = read-only.

Bits [7:4] **Bits 3:0 of coefficient 4 for filter block 1**

These bits contain the four least significant bits of coefficient 4 for filter block 1.

Default = Ch

Bits [3:0] **Reserved**

These bits are reserved.
Default = not applicable

Table 71. REG_COEFF5_BLOCK_1_MS Register (Address = 44h)

7	6	5	4	3	2	1	0
Bits 11:4 of coefficient 5 for filter block 1							
R/W							

LEGEND: R/W = read and write.

Bits [7:0] **Bits 11:4 of coefficient 5 for filter block 1**

These bits contain the eight most significant bits of coefficient 5 for filter block 1.

Default = 0Fh

Table 72. REG_COEFF5_BLOCK_1_LS Register (Address = 45h)

7	6	5	4	3	2	1	0
Bits 3:0 of coefficient 5 for filter block 1				Reserved			
R/W				R			

LEGEND: R/W = read and write; R = read-only.

Bits [7:4] **Bits 3:0 of coefficient 5 for filter block 1**

These bits contain the four least significant bits of coefficient for filter block 1.

Default = 0h

Bits [3:0] **Reserved**

These bits are reserved.
Default = not applicable

Table 73. REG_COEFF6_BLOCK_1_MS Register (Address = 46h)

7	6	5	4	3	2	1	0
Bits 11:4 of coefficient 6 for filter block 1							
R/W							

LEGEND: R/W = read and write.

Bits [7:0] **Bits 11:4 of coefficient 6 for filter block 1**

These bits contain the eight most significant bits of coefficient 6 for filter block 1.

Default = 23h

Table 74. REG_COEFF6_BLOCK_1_LS Register (Address = 47h)

7	6	5	4	3	2	1	0
Bits 3:0 of coefficient 6 for filter block 1				Reserved			
R/W				R			

LEGEND: R/W = read and write; R = read-only.

Bits [7:4] **Bits 3:0 of coefficient 6 for filter block 1**

These bits contain the four least significant bits of coefficient 6 for filter block 1.

Default = Bh

Bits [3:0] **Reserved**

These bits are reserved.
Default = not applicable

Table 75. REG_COEFF7_BLOCK_1_MS Register (Address = 48h)

7	6	5	4	3	2	1	0
Bits 11:4 of coefficient 7 for filter block 1							
R/W							

LEGEND: R/W = read and write.

Bits [7:0] **Bits 11:4 of coefficient 7 for filter block 1**

These bits contain the eight most significant bits of coefficient 7 for filter block 1.

Default = 44h

Table 76. REG_COEFF7_BLOCK_1_LS Register (Address = 49h)

7	6	5	4	3	2	1	0
Bits 3:0 of coefficient 7 for filter block 1				Reserved			
R/W				R			

LEGEND: R/W = read and write; R = read-only.

Bits [7:4] **Bits 3:0 of coefficient 7 for filter block 1**

These bits contain the four least significant bits of coefficient 7 for filter block 1.

Default = 2h

Bits [3:0] **Reserved**

These bits are reserved.
Default = not applicable

Table 77. REG_DAC_SAMPLE_MS Register (Address = 4Ah)

7	6	5	4	3	2	1	0
Bits 11:4 of DAC sample fed from DSP path into DAC							
R/W							

LEGEND: R/W = read and write.

Bits [7:0] **Bits 11:4 of DAC sample fed from DSP path into DAC**

These bits contain the eight most significant bits of DAC sample fed from DSP path into DAC.

Default = 00h

Table 78. REG_DAC_SAMPLE_LS Register (Address = 4Bh)

7	6	5	4	3	2	1	0
Bits 3:0 of DAC sample fed from DSP path into DAC				Reserved			
R/W				R			

LEGEND: R/W = read and write; R = read-only.

Bits [7:4] **Bits 3:0 of DAC sample fed from DSP path into DAC**

These bits contain the four least significant bits of DAC sample fed from DSP path into DAC.

Default = 0h

Bits [3:0] **Reserved**

These bits are reserved.
Default = not applicable

POWER SUPPLIES

The device has two low-voltage analog power-supply pins and one low-voltage digital supply pin. Internally, the two analog supply pins are connected to each other through back-to-back electrostatic discharge (ESD) protection diodes. These pins must be connected to each other on the application printed circuit board (PCB). Connecting the digital supply pin and the two analog supply pins together on the PCB is also recommended. Both low-voltage analog ground pins are also connected internally through back-to-back ESD protection diodes. These ground pins should also be connected to the digital ground pin on the PCB. Bypassing the low-voltage power supplies with a parallel combination of a 10-µF and 100-nF capacitor is recommended. The PA block is biased separately from a high-voltage, high-current supply.

Three PA power-supply pins and three PA ground pins are available to provide a path for the high currents associated with driving the low impedance of the ac mains. Connecting the three PA supply pins together is recommended. Placing a 47-µF to 100-µF bypass capacitor in parallel with a 100-nF capacitor as close as possible to the device is also recommended. Care must be taken when routing the high-current ground lines on the PCB to avoid creating voltage drops in the PCB ground that may vary with changes in load current.

The device has many options to enable or disable the functional blocks to allow for flexible power-savings modes. Refer to the Electrical Characteristics: Power Supply table for power consumption in specific modes.

DAC, SD, INT, TSENSE, TX_FLAG, AND RX_FLAG PINS

This section discusses the DAC, SD, INT, TSENSE, TX_FLAG, and RX_FLAG pins.

DAC (Pin 7)

The DAC pin is used to configure the SPI to either read data to or write data from the command and data registers, or to write data to the DAC register. Setting the DAC pin high allows access to the DAC register. Setting the DAC pin low allows access to the command and data registers.

SD (Pin 8)

The shutdown pin (SD) can be used to shut down the entire device for maximum power savings. When the SD pin is low, the device operates normally. When the SD pin is high, all circuit blocks within the device (including the serial interface) are placed in the lowest-power operating modes. In this condition, the entire device draws only 395 µA (typical) of current. All register contents at the time the device is placed in shutdown mode are erased; when the device is re-enabled, the register contents are the device default values. Follow the protocol described in the External Reset and Analog Shutdown Mode section when asserting the SD pin.

INT (Pin 9)

The interrupt pin (INT) is an active-low, open-drain output pin that can be used to signal the microprocessor of an unusual operating condition that results from an anomaly on the power line. The INT pin can be triggered by external circuit conditions and SPI operations, depending upon the REG_FLAG_CTL register settings. The device can be programmed to issue an interrupt on current overload, thermal overload, and digital error conditions. Refer to the *AFE032 Interrupts* section for more information.

When an interrupt is signaled (that is, INT goes low), the contents of the IFLAG_INT, TFLAG_INT, and DIG_ERR_INT bits (bits 7, 6, and 4, respectively, in the REG_AFE_STATUS register) can be read to determine the type of interrupt that occurred. The REG_FLAG_CTL register settings should be configured each time the device is powered on.

Current overload and thermal overload conditions are explained in the *Current Overload* and *Thermal Overload* sections. Digital error conditions are explained in the *AFE032 Interrupts* section.

Current Overload

The maximum output current allowed from the power amplifier (PA) can be programmed with the external R_{SET} resistor connected between PA_ISET (pin 26) and ground. The PA goes to current limit state if a fault condition occurs, causing the PA to source or sink more current than its programmed limit value. IFLAG_INT (bit 7 in the REG_AFE_STATUS register) is set to '1' if the PA goes to current limit state for more than 16,384 DAC_CLK cycles.

Setting the IFLAG mask bit of the REG_FLAG_CTL register prevents a fault condition from commanding the active-low, open-drain interrupt pin (INT). Note that the PA still goes to a current limit state to protect the device and the IFLAG_INT bit is still set to '1'.

CAUTION

ENPAICLN and ENPAICLP (bits 1 and 0 of the REG_PA_CURRENT_CFG register, respectively) allow the current limit protection circuitry to be enabled or disabled. By default, the current limit protection circuitry is enabled and protects the device from damage during current overload events only if the ENPAICLN and ENPAICLP bits remain in their default states. Disabling these bits can potentially damage the device in an current overload event.

Thermal Overload

The device contains internal PA thermal shutdown protection circuitry that automatically disables the PA output stage if the junction temperature exceeds +165°C.

Note that the thermal shutdown protection circuitry only operates if a fault condition causes thermal overload (that is, forces the junction temperature to exceed +165°C) and the Disable TLIM bit (bit 0 in the REG_DAC/HPF/LPF/PA_CTL register) remains in the default state of '0'. The device thermal shutdown protection circuitry allows the PA to resume normal operation only when the junction temperature falls below +150°C. The TFLAG_INT bit remains set to '1' even after the device returns to normal operation. The TFLAG_INT bit can be reset to '0' by performing a read operation on the REG_AFE_STATUS register.

Setting the TFLAG mask bit of the REG_FLAG_CTL register prevents a thermal overload event from commanding the active-low, open-drain interrupt pin (INT). Note that the internal PA thermal shutdown protection circuitry still disables the PA output stage automatically (provided that a thermal overload condition occurs and the Disable TLIM bit is in set to '0') and the TFLAG_INT bit is still set to '1'.

TSENSE (Pin 35)

The TSENSE pin is internally connected to the anode of a temperature-sensing diode located within the PA output stage. Figure 26 shows a remote junction temperature sensor circuit that can be used to measure the device junction temperature. Measuring the device junction temperature is optional and is not required.

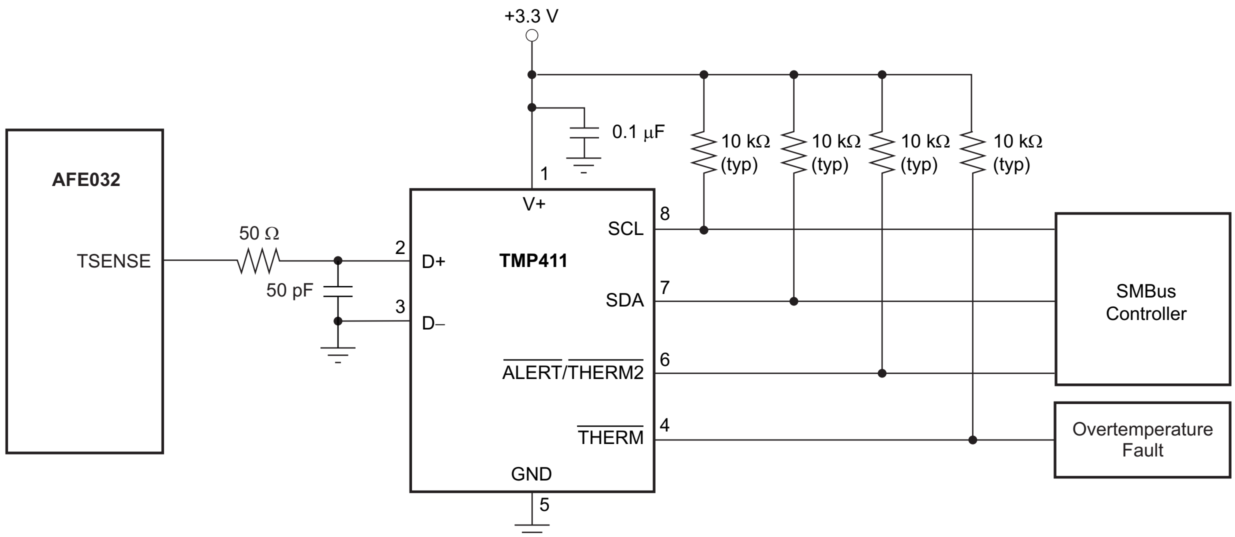


Figure 26. Interfacing the TMP411 to the AFE032

TX_FLAG (Pin 47)

The TX_FLAG pin is an open-drain output that indicates the readiness of the Tx signal path for transmission. When the TX_FLAG pin is high, the transmit signal path is enabled and ready for transmission. When the TX_FLAG pin is low, the transmit path is not ready for transmission.

RX_FLAG (Pin 48)

The RX_FLAG pin is an open-drain output that indicates the readiness of the Rx signal path for transmission. When the RX_FLAG pin is high, the transmit signal path is enabled and ready for transmission. When the RX_FLAG pin is low, the transmit path is not ready for transmission.

LINE-COUPLING CIRCUIT

The line-coupling circuit is one of the most critical circuits in a power-line modem. The line-coupling circuit has two primary functions: first, to block the low-frequency signal of the mains (commonly 50 Hz or 60 Hz) from damaging the low-voltage modem circuitry; second, to couple the modem signal to and from the ac mains. A typical line-coupling circuit is shown in Figure 27.

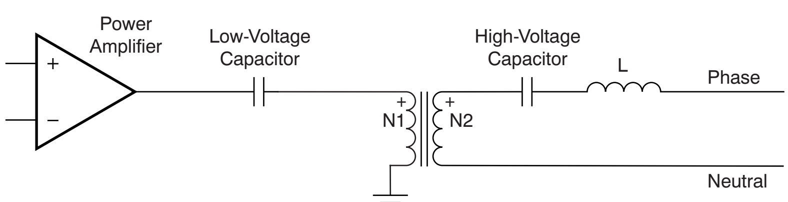


Figure 27. Simplified Line-Coupling Circuit

CIRCUIT PROTECTION

Power-line communications are often located in operating environments that are harsh for electrical components connected to the ac line. Noise or surges from electrical anomalies (such as lightning, capacitor bank switching, inductive switching, or other grid fault conditions) can damage high-performance integrated circuits if proper protection is not provided. The AFE032, however, can survive even the harshest conditions by using a variety of techniques to protect the device.

Layout the protection circuitry in order to dissipate as much of the electrical disturbance as possible with a multi-layer approach using metal-oxide varistors (MOVs), transient voltage suppression diodes (TVSs), Schottky diodes, and a Zener diode. These components dissipate the electrical disturbance before the anomaly reaches the device. Figure 28 shows the recommended strategy for transient overvoltage protection.

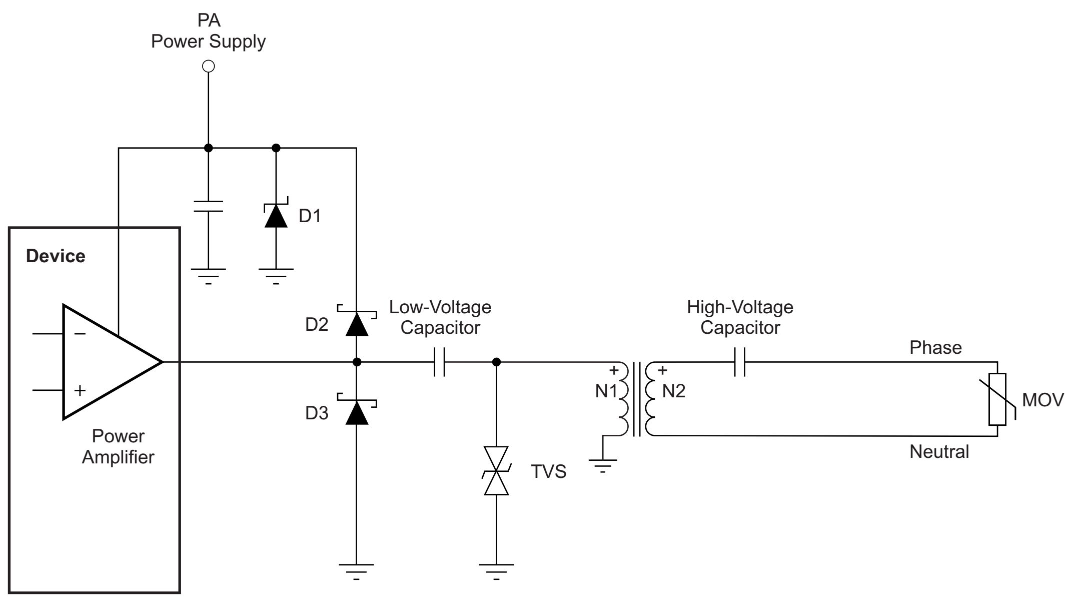


Figure 28. Transient Overvoltage Protection for AFE032

Note that the high-voltage coupling capacitor must be able to withstand pulses up to the clamping protection provided by the MOV. A metalized polypropylene capacitor, such as the 474MKP275KA from Illinois Capacitor™, is rated for 50 Hz to 60 Hz and 250 VAC to 310 VAC, and can withstand 24 impulses of 2.5 kV.

Table 79 and Table 80 list several recommended transient protection components.

Table 79. Recommended Transient Protection Devices (120 VAC, 60 Hz)

COMPONENT	DESCRIPTION	MANUFACTURER	MFR PART NO (OR EQUIVALENT)
D1	Zener diode	Diodes, Inc.	1SMB59xxB(1)
D2, D3	Schottky diode	Diodes, Inc.	B340A
TVS	Transient voltage suppressor	Littelfuse, Inc.	SMCJxxCA(2)
MOV	Varistor	Littelfuse, Inc.	TMOV20RP140E
HV capacitor	High-voltage capacitor	Illinois Capacitor, Inc	474MKP275KA(3)

(1) Select the zener breakdown voltage at the lowest available rating beyond the normal power-supply operating range. For example, 1SMB5931B is suitable for systems where PA_VS = 15 V, whereas 1SMB5934B is suitable for systems where PA_VS = 20 V.
(2) Select the TVS breakdown voltage at or slightly less than (0.5 × PA_VS). For example, SMCJ6.0CA is suitable for systems where PA_VS = 15 V, whereas SMCJ8.0CA is suitable for systems where PA_VS = 20 V.
(3) A common value for the high-voltage capacitor is 470 nF. Other values may be substituted depending on the appliction requirements. Note that when making a substitution, for reliability, the capacitor must be selected from the same family or an equivalent family of capacitors rated to withstand high-voltage surges on the power line.

Table 80. Recommended Transient Protection Devices (240 VAC, 50 Hz)

COMPONENT	DESCRIPTION	MANUFACTURER	MFR PART NO (OR EQUIVALENT)
D1	Zener diode	Diodes, Inc.	1SMB59xxB(1)
D2, D3	Schottky diode	Diodes, Inc.	B340A
TVS	Transient voltage suppressor	Littelfuse, Inc.	SMCJxxCA(2)
MOV	Varistor	Littelfuse, Inc.	TMOV20RP300E
HV capacitor	High-voltage capacitor	Illinois Capacitor, Inc	474MKP275KA(3)

(1) Select the zener breakdown voltage at the lowest available rating beyond the normal power-supply operating range. For example, 1SMB5931B is suitable for systems where PA_VS = 15 V, whereas 1SMB5934B is suitable for systems where PA_VS = 20 V.
(2) Select the TVS breakdown voltage at or slightly less than (0.5 × PA_VS). For example, SMCJ6.0CA is suitable for systems where PA_VS = 15 V, whereas SMCJ8.0CA is suitable for systems where PA_VS = 20 V.
(3) A common value for the high-voltage capacitor is 470 nF. Other values may be substituted depending on the appliction requirements. Note that when making a substitution, for reliability, the capacitor must be selected from the same family or an equivalent family of capacitors rated to withstand high-voltage surges on the power line.

THERMAL CONSIDERATIONS

In a typical power-line communications application, the device dissipates 2 W of power when transmitting to the low-impedance ac line. This amount of power dissipation can increase the junction temperature, which in turn can lead to a thermal overload that results in signal transmission interruptions if the PCB thermal design is not implemented properly. Proper management of heat flow from the device as well as good PCB design and construction are required to ensure proper device temperature, maximize performance, and extend device operating life.

The device is assembled in a 7-mm x 7-mm, QFN-48 package. As Figure 29 shows, this QFN package has a large-area exposed thermal pad on the underside that is used to conduct heat away from the device and to the underlying PCB.

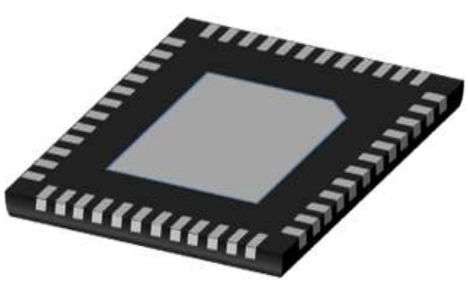


Figure 29. QFN Package with Large-Area Exposed Thermal Pad

Some heat is conducted from the silicon die surface through the plastic packaging material and is transferred to the ambient environment. However, this route is not the primary thermal path for heat flow because plastic is a relatively poor conductor of heat. Heat also flows across the silicon die surface to the bond pads, through the wire bonds, to the package leads, and finally to the top layer of the PCB. While both of these paths for heat flow are important, the majority (nearly 80%) of the heat flows downward, through the silicon die, to the thermally-conductive die-attach epoxy, and to the exposed thermal pad on the underside of the package (as shown in Figure 30). Minimizing the thermal resistance of this downward path to the ambient environment maximizes the life and performance of the device.

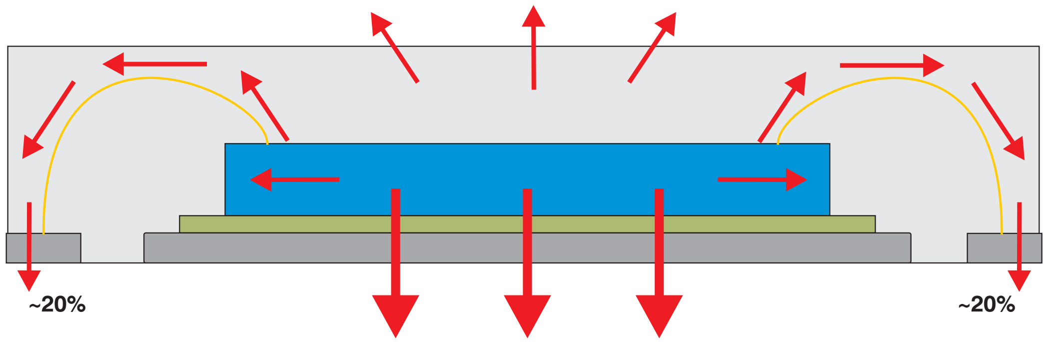


Figure 30. Heat Flow in the QFN Package

The exposed thermal pad must be soldered to the PCB thermal pad. The thermal pad on the PCB must be the same size as the exposed thermal pad on the underside of the QFN package. Refer to Application Report, *QFN/SON PCB Attachment* (SLUA271A), for recommendations on attaching the thermal pad to the PCB. Figure 31 illustrates the direction of heat spreading to the PCB from the device.

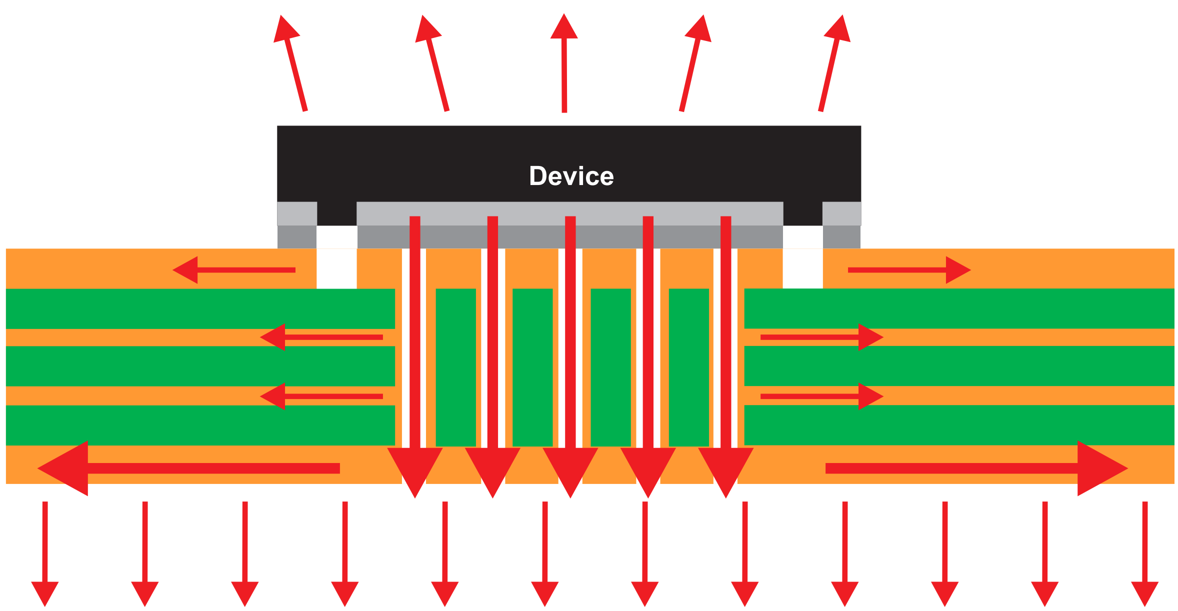


Figure 31. Heat Spreading to PCB

The heat spreading to the PCB is maximized if the thermal path is uninterrupted. Best results are achieved if the heat-spreading surfaces are filled with copper to the greatest extent possible, thus maximizing the percentage of area covered on each layer. As an example, a thermally robust, multilayer PCB design can consist of four layers with copper (Cu) coverage of 60% in the top layer, 85% and 90% in the inner layers (respectively), and 95% on the bottom layer.

Increasing the number of layers in the PCB, using thicker copper, and increasing the PCB area are all factors that improve the spread of heat. Figure 32 through Figure 34 show thermal resistance performance as a function of each of these factors.

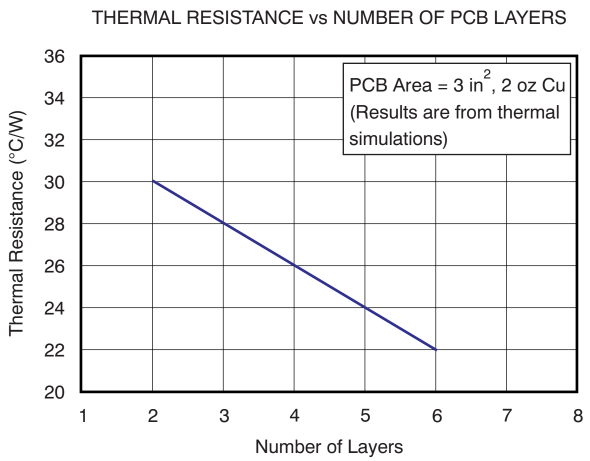


Figure 32. Thermal Resistance as a Function of the Number of Layers in the PCB

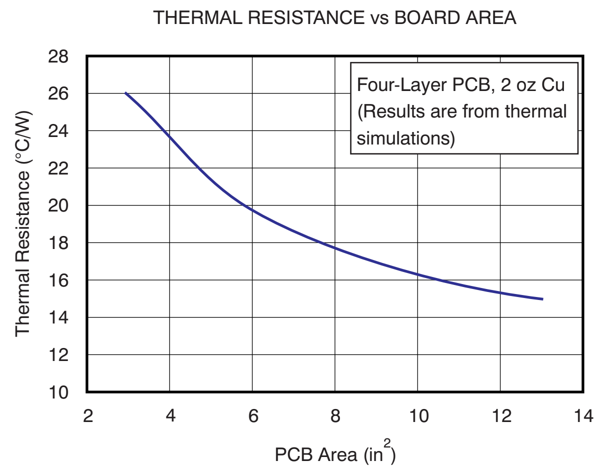


Figure 33. Thermal Resistance as a Function of PCB Area

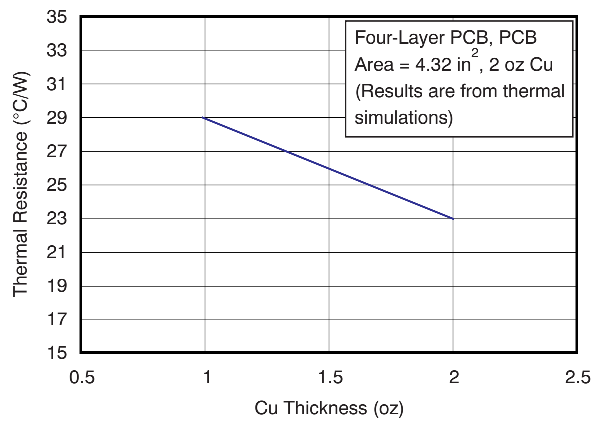


Figure 34. Thermal Resistance as a Function of Copper Thickness

For additional information on thermal PCB design using exposed thermal pad packages, refer to Application Reports *Analog Front-End Design for a Narrowband Power-Line Communications Modem Using the AFE031* (SBOA130) and *PowerPAD™ Thermally-Enhanced Package* (SLMA002E) (both available for download at www.ti.com).

TYPICAL APPLICATION SCHEMATIC

A schematic for a typical application is provided in Figure 35.

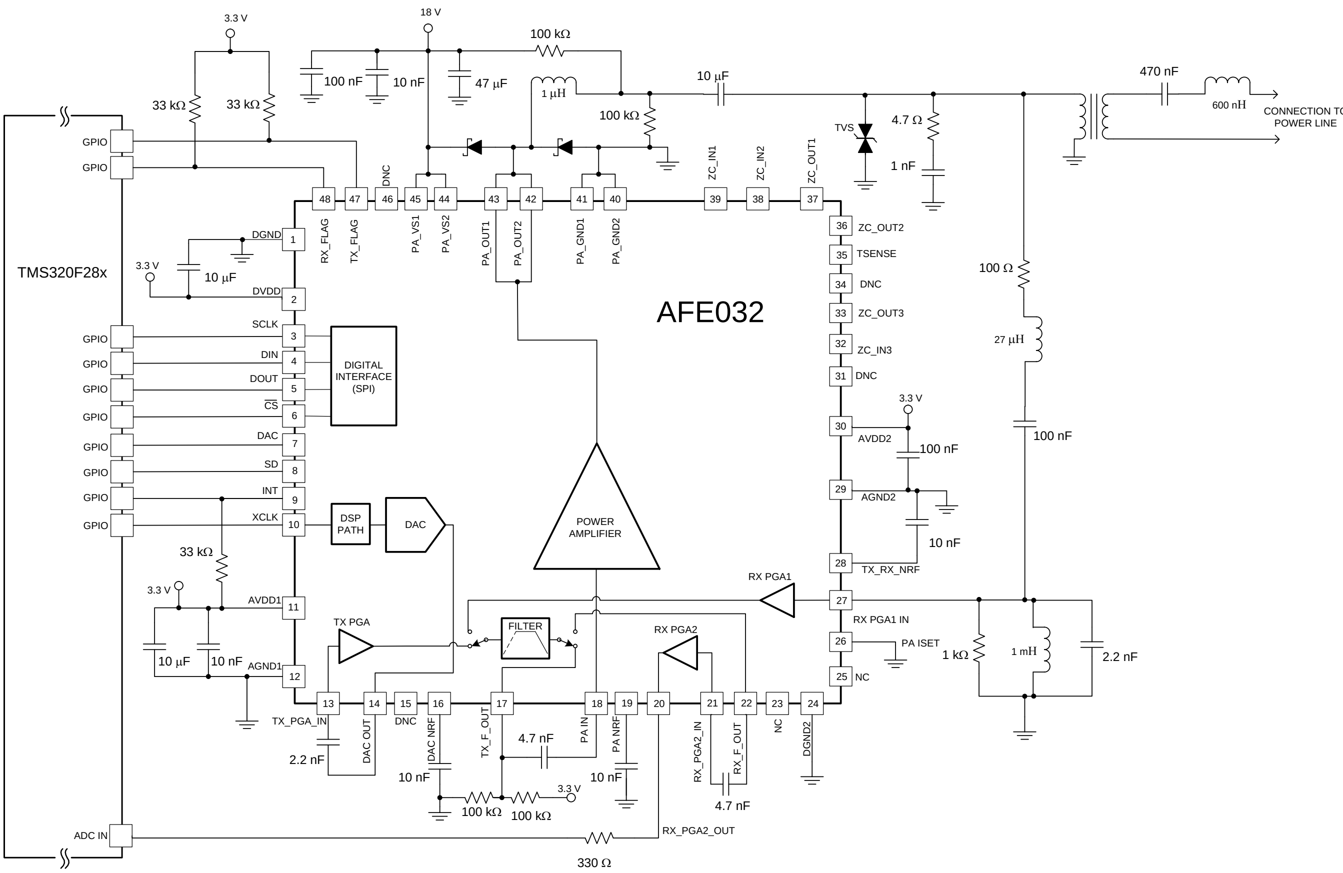


Figure 35. Typical Application with Transformer Coupling

PACKAGING AND MECHANICALS

Complete mechanical drawings and packaging information are appended to the end of this data sheet.

修订历史记录

请注意：前一修订版的页码可能与当前版本的页码不同。

Changes from Original (August 2013) to Revision A — Page

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
AFE032IRGZR	ACTIVE	VQFN	RGZ	48	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 125	AFE032	Samples
AFE032IRGZT	ACTIVE	VQFN	RGZ	48	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 125	AFE032	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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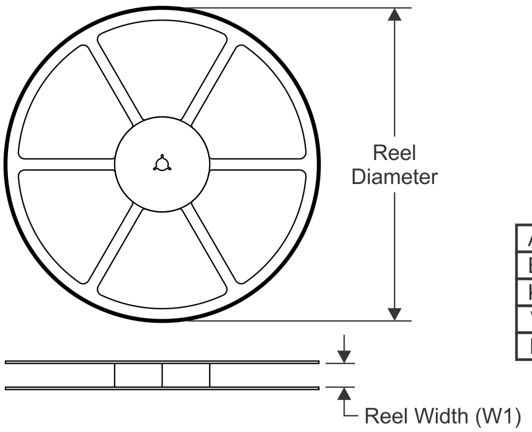
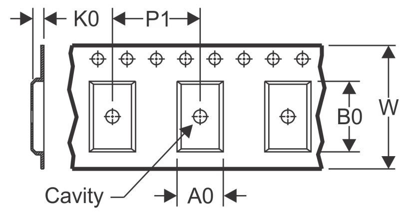
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

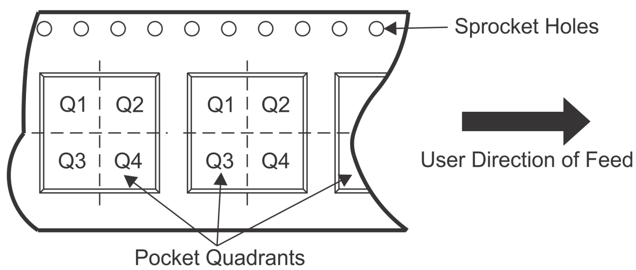


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

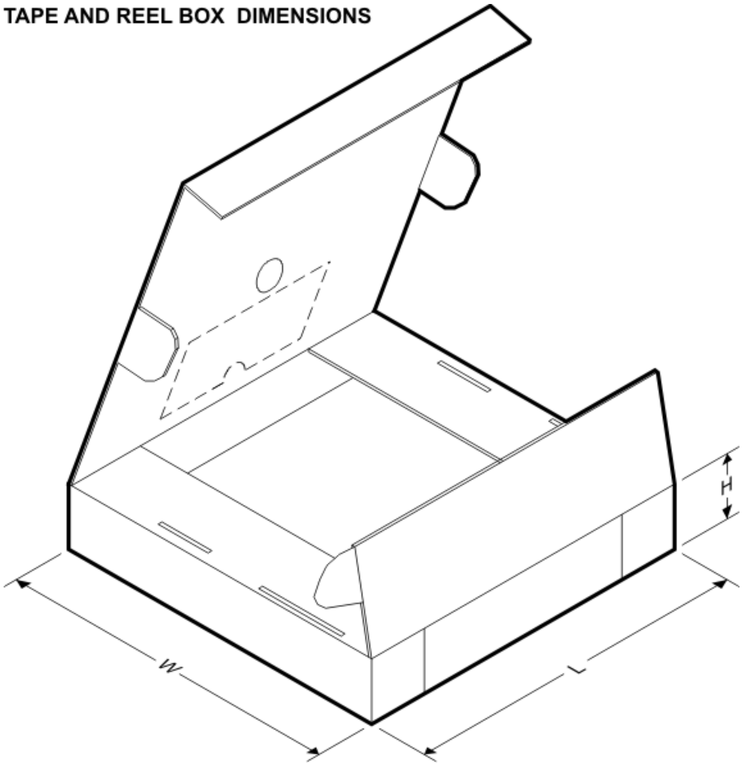
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AFE032IRGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
AFE032IRGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

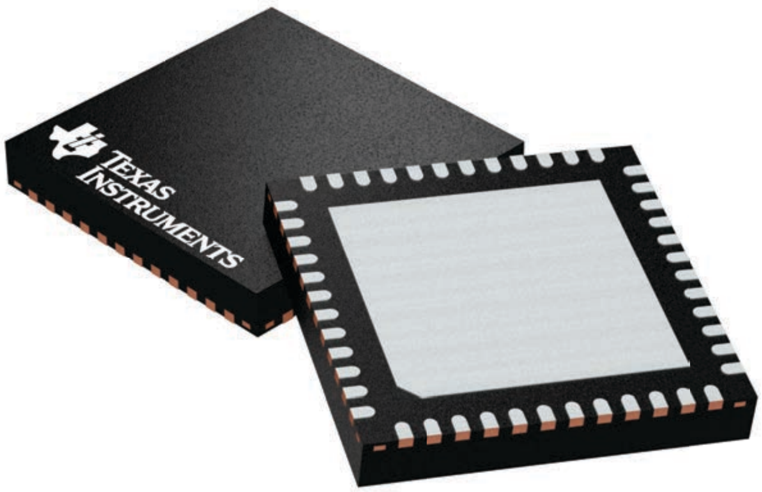
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AFE032IRGZR	VQFN	RGZ	48	2500	367.0	367.0	38.0
AFE032IRGZT	VQFN	RGZ	48	250	210.0	185.0	35.0

RGZ 48

VQFN - 1 mm max height

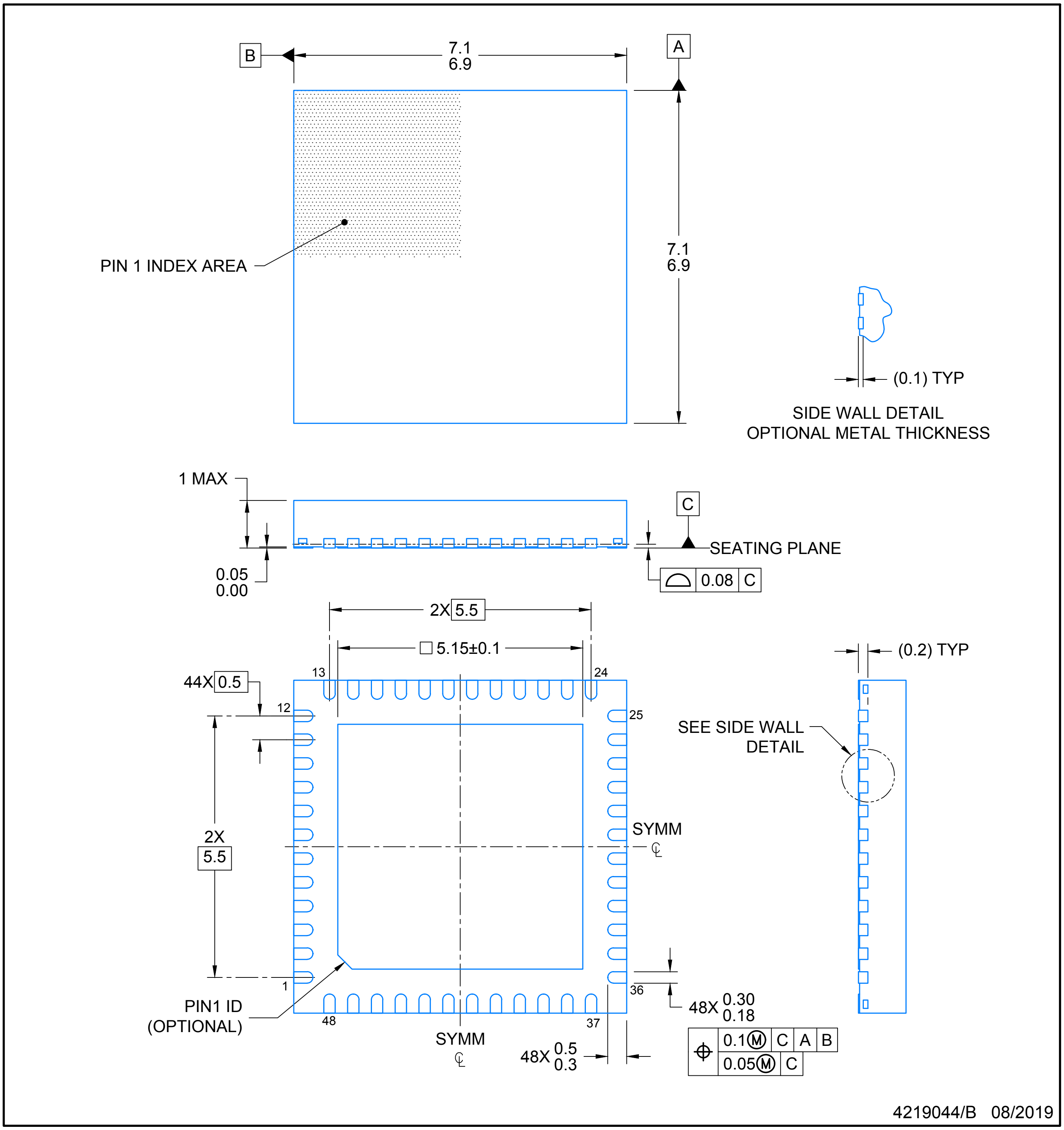
7 x 7, 0.5 mm pitch

PLASTIC QUADFLAT PACK- NO LEAD



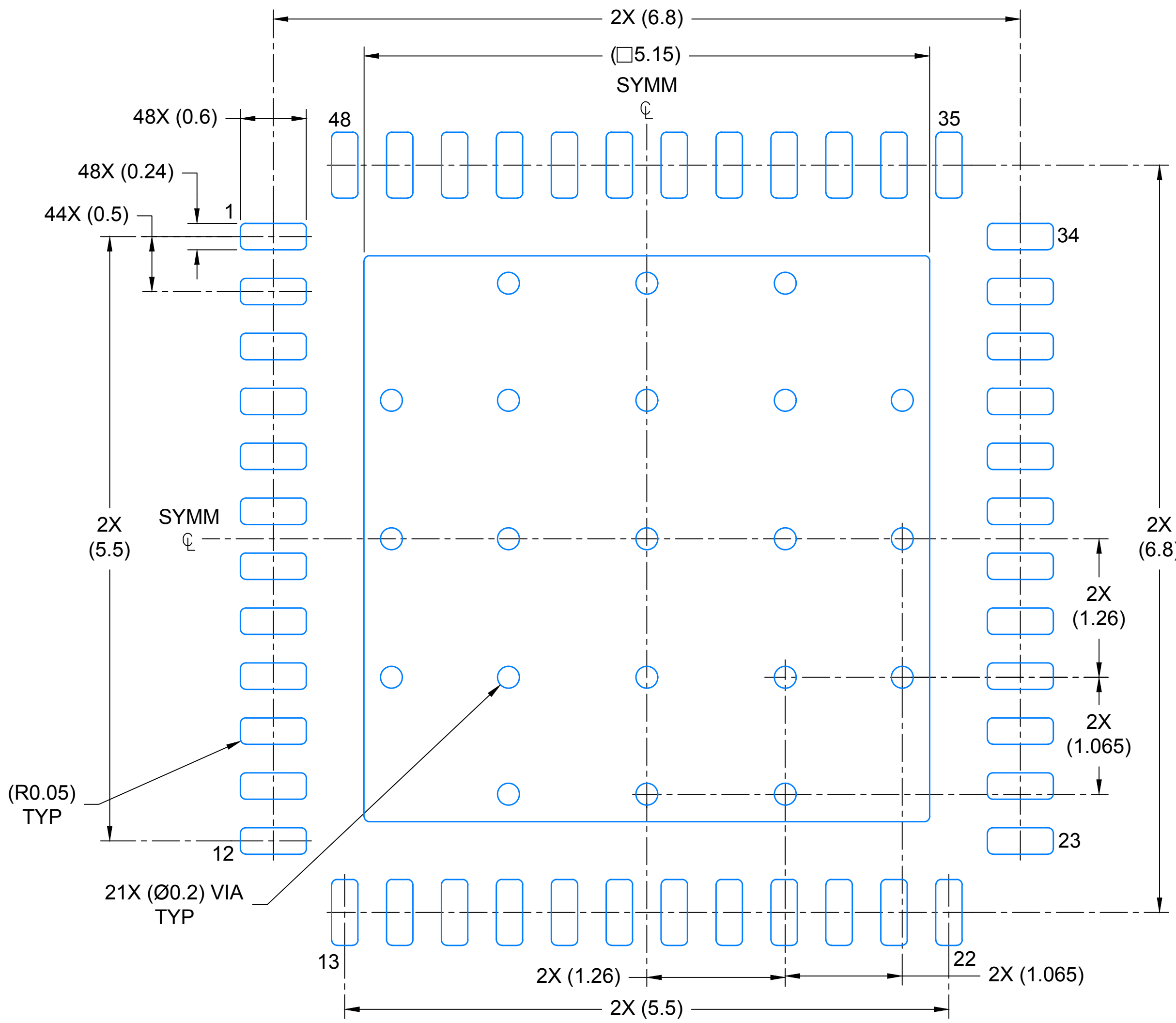
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224671/A

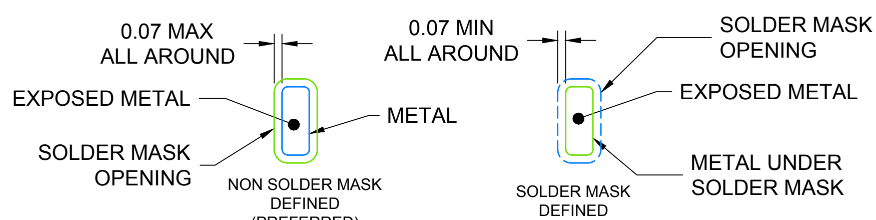


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE: 15X

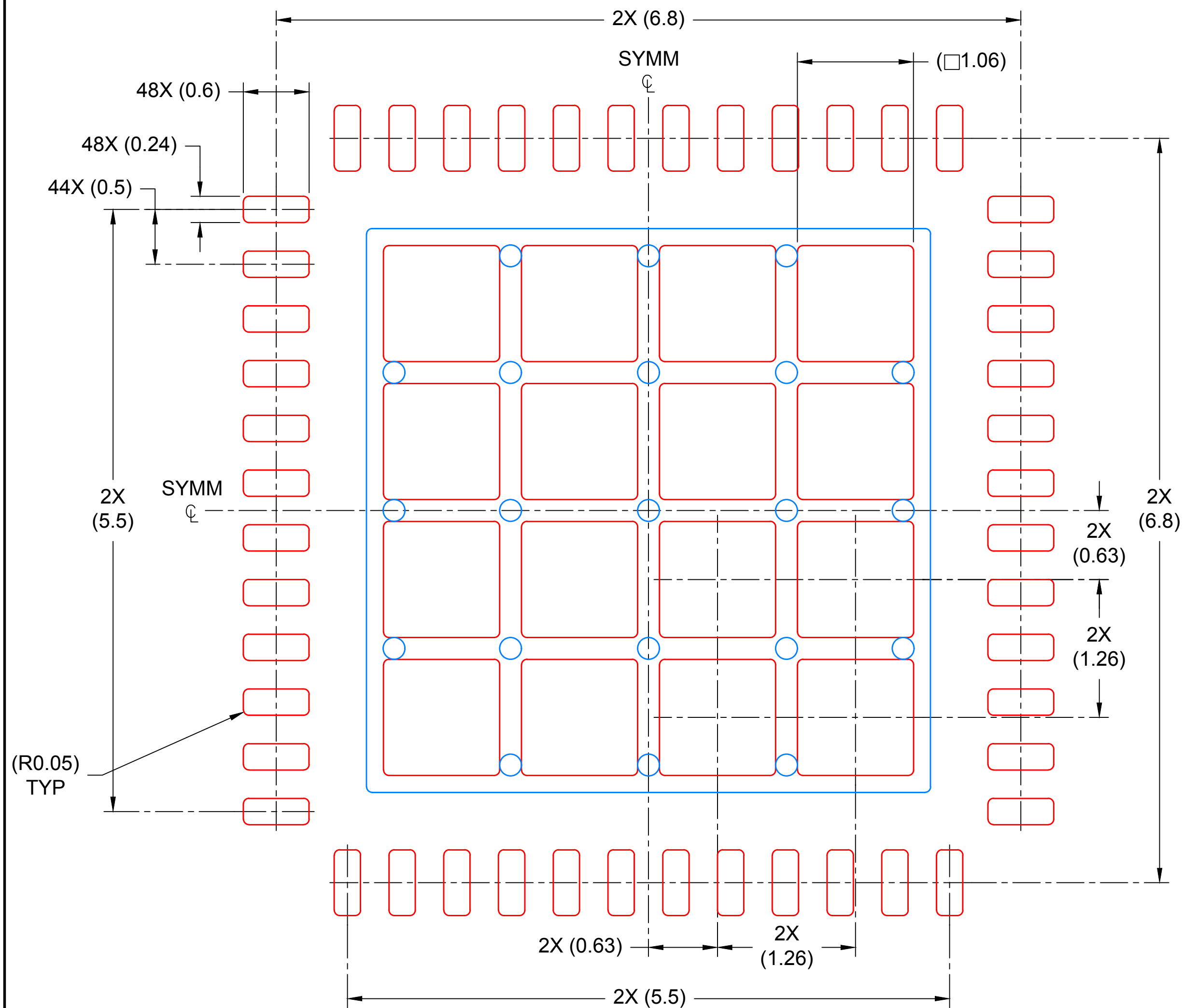


SOLDER MASK DETAILS

4219044/B 08/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
67% PRINTED COVERAGE BY AREA
SCALE: 15X

4219044/B 08/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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