HIGH EFFICIENCY CLASS-G ADSL LINE DRIVER

FEATURES

- **Low Total Power Consumption Increases ADSL Line Card Density (20 dBm on Line)**
  - **600 mW w/Active Termination (Full Bias)**
  - **530 mW w/Active Termination (Low Bias)**
- **Low MTPR of –74 dBc (All Bias Conditions)**
- **High Output Current of 500 mA (typ)**
- **Wide Supply Voltage Range of ±5 V to ±15 V [$V_{CC(H)}$] and ±3.3 V to ±15 V [$V_{CC(L)}$]**
- **Wide Output Voltage Swing of 43 Vpp Into 100-Ω Differential Load [$V_{CC(H)}$ = ±12 V]**
- **Multiple Bias Modes Allow Low Quiescent Power Consumption for Short Line Lengths**
  - **160-mW/ch Full Bias Mode**
  - **135-mW/ch Mid Bias Mode**
  - **110-mW/ch Low Bias Mode**
  - **75-mW/ch Terminate Only Mode**
  - **13-mW/ch Shutdown Mode**
- **Low Noise for Increased Receiver Sensitivity**
  - **3.3 pA/√Hz Noninverting Current Noise**
  - **9.5 pA/√Hz Inverting Current Noise**
  - **3.5 nV/√Hz Voltage Noise**

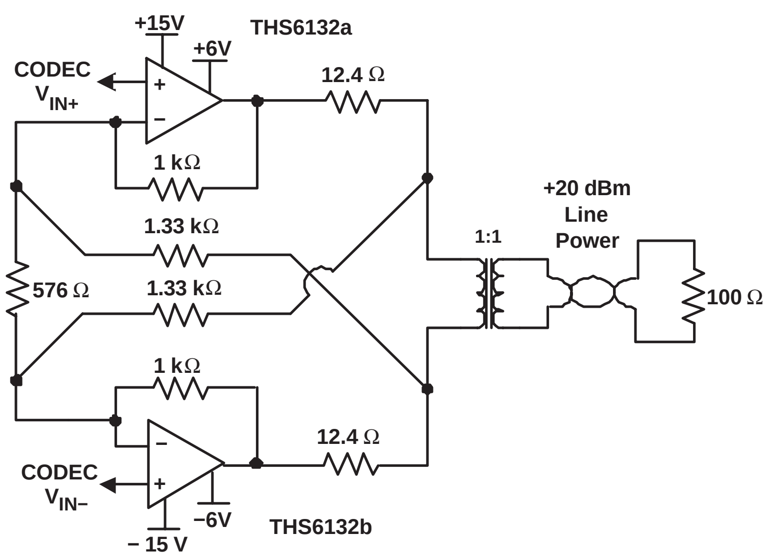
APPLICATIONS

- **Ideal for Active Termination Full Rate ADSL DMT applications (20-dBm Line Power)**

DESCRIPTION

The THS6132 is a Class-G current feedback differential line driver ideal for full rate ADSL DMT systems. Its extremely low power consumption of 600 mW or lower is ideal for ADSL systems that must achieve high densities in ADSL central office rack applications. The unique patent pending architecture of the THS6132 allows the quiescent current to be much lower than existing line drivers while still achieving very high linearity. In addition, the multiple bias settings of the amplifiers allow for even lower power consumption for line lengths where the full performance of the amplifier is not required. The output voltage swing has been vastly improved over first generation Glass-G amplifiers and allows the use of lower power supply voltages that help conserve power. For maximum flexibility, the THS6132 can be configured in classical Class-AB mode requiring only as few as one power supply.

Typical ADSL CO Line Driver Circuit Utilizing Active Impedance Supporting A 6.3 Crest Factor



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage.

ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE CODE	SYMBOL	T_A	ORDER NUMBER	TRANSPORT MEDIA
THS6132VFP	TQFP-32 PowerPAD™	VFP−32	THS6132	−40°C to 85°C	THS6132VFP	Tube
					THS6132VFPR	Tape and reel
THS6132RGW	Leadless 25-pin 5,mm x 5, mm PowerPAD™	RGW−25	6132		THS6132RGWR	Tape and reel

PACKAGE DISSIPATION RATINGS

PACKAGE	Θ_{JA}	Θ_{JC}	$T_A \leq 25°C$ POWER RATING(1)	$T_A = 70°C$ POWER RATING(1)	$T_A = 85°C$ POWER RATING(1)
VFP−32	29.4°C/W	0.96°C/W	3.57 W	2.04 W	1.53 W
RGW−25	31°C/W	1.7°C/W	3.39 W	1.94 W	1.45 W

(1) Power rating is determined with a junction temperature of 130°C. This is the point where distortion starts to substantially increase. Thermal management of the final PCB should strive to keep the junction temperature at or below 125°C for best performance.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

		THS6132
Supply voltage, $V_{CC(H)}$ and $V_{CC(L)}$ (2)		±16.5 V
Input voltage, V_I		$\pm V_{CC(L)}$
Output current, I_O (3)		900 mA
Differential input voltage, V_{IO}		±2 V
Maximum junction temperature, T_J (see Dissipation Rating Table for more information)		150°C
Operating free−air temperature, T_A		−40°C to 85°C
Storage temperature, T_{Stg}		65°C to 150°C
Lead temperature, 1,6 mm (1/16−inch) from case for 10 seconds		300°C
ESD ratings	HBM	1 kV
	CDM	500 V
	MM	200 V

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) $V_{CC(H)}$ must always be greater than or equal to $V_{CC(L)}$ for proper operation. Class-AB mode operation occurs when $V_{CC(H)}$ is equal to VCC(L) and is considered acceptable operation for the THS6132 even though it is not fully specified in this mode of operation.

(3) The THS6132 incorporates a PowerPAD on the underside of the chip. This acts as a heatsink and must be connected to a thermally dissipating plane for proper power dissipation. Failure to do so may result in exceeding the maximum junction temperature that could permanently damage the device. See TI Technical Brief SLMA002 for more information about utilizing the PowerPAD thermally enhanced package.

PowerPAD is a trademark of Texas Instruments.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply voltage	$+V_{CC(H)}$ to $-V_{CC(H)}$	$\pm V_{CC(L)}$	±15	±16	V
	$+V_{CC(L)}$ to $-V_{CC(L)}$	±3.3	±5	$\pm V_{CC(H)}$	
Operating free-air temperature, T_A		−40		85	°C

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range, T_A = 25°C,$V_{CC(H)}$ = ±15 V, $V_{CC(L)}$ = ±5 V R_F = 1.5 kΩ, Gain = +10, Full Bias Mode, R_L = 50 Ω (unless otherwise noted)

	PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
NOISE/DISTORTION PERFORMANCE								
	Multitone power ratio		Gain =+11, 163kHz to 1.1MHz DMT, +20 dBm Line Power, 1:1.1 transformer, active termination, synthesis factor = 4			−74		dBc
	Receive band spill-over		Gain =+11, 25 kHz to 138 kHz with MTPR signal applied			−95		dBc
HD	Harmonic distortion (Differential Configuration, f = 1 MHz, $V_{O(PP)}$ = 2 V, Gain = +10)		2nd harmonic	Differential load = 100 Ω		−84		dBc
				Differential load = 25 Ω		−69		
			3rd harmonic	Differential load = 100 Ω		−92		dBc
				Differential load = 25 Ω		−73		
V_n	Input voltage noise		f = 10 kHz			3.5		nV/√Hz
I_n	Input current noise	+Input	f = 10 kHz			3.3		pA/√Hz
		−Input				9.5		
	Crosstalk		f = 1 MHz, R_L = 100 Ω,	$V_{O(PP)}$ = 2 V, Gain = +2		−52		dBc
OUTPUT CHARACTERISTICS								
V_O	Single−ended output voltage swing		$V_{CC(H)}$ = ±12 V	R_L = 100 Ω	±10.4	±10.8		V
				R_L = 30 Ω	±9.9	±10.4		
			$V_{CC(H)}$ = ±15 V	R_L = 100 Ω	±13.3	±13.8		V
				R_L = 50 Ω	±13	±13.6		
	Output voltage transition from $V_{CC(L)}$ to $V_{CC(H)}$ (Point where $I_{CC(L)} = I_{CC(H)}$)		R_L = 50 Ω	$V_{CC(L)}$ = ±5 V		±3.1		V
				$V_{CC(L)}$ = ±6 V		±3.9		
I_O	Output current (1)		R_L = 10 Ω	$V_{CC(H)}$ = ±12 V		±500		mA
				$V_{CC(H)}$ = ±15 V	±400	±500		
$I_{(SC)}$	Short-circuit current (1)		R_L = 1 Ω	$V_{CC(H)}$ = ±15 V		±750		mA
	Output resistance		Open-loop			5		Ω
	Output resistance—terminate mode		f = 1 MHz,	Gain = +10		0.35		Ω
	Output resistance—shutdown mode		f = 1 MHz,	Open-loop		5.5		kΩ

(1) A heatsink is required to keep the junction temperature below absolute maximum rating when an output is heavily loaded or shorted. See Absolute Maximum Ratings section for more information.

ELECTRICAL CHARACTERISTICS (continued)

over recommended operating free-air temperature range, T_A = 25°C, $V_{CC(H)}$ = ±15 V, $V_{CC(L)}$ = ±5 V R_F = 1.5 kΩ, Gain = +10, Full Bias Mode, R_L = 50 Ω (unless otherwise noted)

POWER SUPPLY

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{CC(x)}$	Operating range	$\pm V_{CC(H)}$		$\pm V_{CC(L)}$	±15	±16.5	V
		$\pm V_{CC(L)}$		±3	±5	$\pm V_{CC(H)}$	
I_{CC}	Quiescent current (each driver) Full-bias mode (Bias−1 = 1, Bias−2 = 1, Bias−3 = X) (Icc trimmed with $V_{CC(H)}$ = ±15 V, $V_{CC(L)}$ = ±5 V)	$V_{CC(L)}$ = ±5 V; ($V_{CC(H)}$= ±15 V)	T_A = 25°C	5.7	6.4	7.5	mA
			T_A = full range			8.1	
		$V_{CC(L)}$ = ±6 V; ($V_{CC(H)}$ = ±15 V)	T_A = 25°C		6.7		mA
			T_A = full range				
		$V_{CC(H)}$ = ±12 V; ($V_{CC(L)}$ = ±5 V)	T_A = 25°C		3.1		mA
			T_A = full range				
		$V_{CC(H)}$ = ±15 V; ($V_{CC(L)}$ = ±5 V)	T_A = 25°C	2.9	3.25	3.75	mA
			T_A = full range			4.25	
	Quiescent current (each driver) Variable bias modes, $V_{CC(L)}$ = ±5 V	Mid; Bias−1 = 1, Bias−2 = 0, Bias−3 = 1		5.0	5.6	6.8	mA
		Low; Bias−1 = 1, Bias−2 = 0, Bias−3 = 0		4.25	4.8	6.0	
		Terminate; Bias−1 = 0, Bias−2 = 1, Bias−3 = X(1)		3.2	3.8	4.5	
		Shutdown; Bias−1 = 0, Bias−2 = 0, Bias−3 = X(1)			1	1.3	
	Quiescent current (each driver) Variable bias modes, $V_{CC(H)}$ = ±15 V	Mid; Bias−1 = 1, Bias−2 = 0, Bias−3 = 1		2.4	2.7	3.0	mA
		Low ; Bias−1 = 1, Bias−2 = 0, Bias−3 = 0		1.9	2.15	2.4	
		Terminate; Bias−1 = 0, Bias−2 = 1, Bias−3 = X(1)		1.1	1.3	1.5	
		Shutdown ; Bias−1 = 0, Bias−2 = 0, Bias−3 = X(1)			0.1	0.5	
PSRR	Power supply rejection ratio ($\Delta V_{CC(x)}$ = ±1 V)	$V_{CC(L)}$ = ±5V	T_A = 25°C	−70	−82		dB
			T_A = full range	−68			
		$V_{CC(H)}$ = ±15V	T_A = 25°C	−70	−82		
			T_A = full range	−68			

(1) X is used to denote a logic state of either 1 or 0.

ELECTRICAL CHARACTERISTICS (continued)

over recommended operating free-air temperature range, T_A = 25°C,$V_{CC(H)}$ = ±15 V, $V_{CC(L)}$ = ±5 V R_F = 1.5 kΩ, Gain = +10, Full Bias Mode, R_L = 50 Ω (unless otherwise noted)

DYNAMIC PERFORMANCE

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
BW	Single-ended small-signal bandwidth (−3 dB), V_O = 0.1 Vrms	R_L = 100 Ω	Gain = +1, RF = 750 Ω		80		MHz
			Gain = +2, RF = 620 Ω		70		
			Gain = +5, RF = 500 Ω		60		
			Gain = +10, RF = 1 kΩ		20		
		R_L = 25 Ω	Gain = +1, RF = 750 Ω		60		MHz
			Gain = +2, RF = 620 Ω		55		
			Gain = +5, RF = 500 Ω		50		
			Gain = +10, RF = 1 kΩ		17		
SR	Single-ended slew-rate(1)	V_O = 20 V_{PP},	Gain =+10		300		V/µs

(1) Slew-rate is defined from the 25% to the 75% output levels

DC PERFORMANCE

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OS}	Input offset voltage	$V_{CC(L)}$ = ± 5 V, ±6 V	T_A = 25°C		1	15	mV
			T_A = full range			20	
	Differential offset voltage		T_A = 25°C		0.3	6	
			T_A = full range			8	
	Offset drift		T_A = full range		40		µV/°C
I_{IB}	−Input bias current	$V_{CC(L)}$ = ±5 V, ±6 V	T_A = 25°C		1	15	µA
			T_A = full range			20	
	+ Input bias current		T_A = 25°C		1.5	15	
			T_A = full range			20	
Z_{OL}	Open loop transimpedance	R_L = 1 kΩ			2		MΩ

ELECTRICAL CHARACTERISTICS (continued)

over recommended operating free-air temperature range, T_A = 25°C,$V_{CC(H)}$ = ±15 V, $V_{CC(L)}$ = ±5 V R_F = 1.5 kΩ, Gain = +10, Full Bias Mode, R_L = 50 Ω (unless otherwise noted)

INPUT CHARACTERISTICS

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{ICR}	Input common−mode voltage range(1)	$V_{CC(L)}$ = ±5 V	T_A = 25°C	±2.7	±3.0		V
			T_A = full range	±2.6			
		$V_{CC(L)}$ = ±6 V	T_A = 25°C		±4.0		
	REF pin input voltage range	$V_{CC-(L)}$= ±5 V			±2.5		V
		$V_{CC(L)}$ = ±6 V			±3.5		
CMRR	Common-mode rejection ratio	$V_{CC(L)}$ = ±5 V, ±6 V	T_A = 25°C	60	67		dB
			T_A = full range	57			
R_I	Input resistance	+ Input			800		kΩ
		− Input			45		Ω
C_I	Differential Input capacitance				1.2		pF

(1) To conserve as much power as possible, the input stage of the THS6132 is powered from the $V_{CC(L)}$ supplies and is limited by the $V_{CC(L)}$ supply voltage. For Class-AB operation, connect the $V_{CC(L)}$ supplies to $V_{CC(H)}$.

LOGIC CONTROL CHARACTERISTICS

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	Bias pin voltage for logic 1	Relative to DGND pin voltage	2.0			V
V_{IL}	Bias pin voltage for logic 0	Relative to DGND pin voltage			0.8	V
I_{IH}	Bias pin current for logic 1	V_{IH} = 5 V, DGND = 0 V		−0.1	−0.2	µA
I_{IL}	Bias pin current for logic 0	V_{IL} = 0 V, DGND = 0 V		−0.1	−0.2	µA
	Transition time—logic 0 to logic 1(1)			0.1		µs
	Transition time—logic 1 to logic 0(1)			0.2		µs
	DGND useable range		$-V_{CC(H)}$		$+V_{CC(H)}$ −5	V

(1) Transition time is defined as the time from when the logic signal is applied to the time when the supply current has reached half its final value.

LOGIC TABLE

BIAS-1	BIAS-2	BIAS-3	FUNCTION	DESCRIPTION
1	1	X(1)	Full bias mode	Amplifiers ON with lowest distortion possible
1	0	1	Mid bias mode	Amplifiers ON with power savings with a reduction in distortion performance
1	0	0	Low bias mode	Amplifiers ON with enhanced power savings and a reduction of distortion performance
0	1	X(1)	Terminate mode	Lowest power state with +Vin pins internally connect to REF pin and output has low impedance
0	0	X(1)	Shutdown mode	Amplifiers OFF and output has high impedance

(1) X is used to denote a logic state of either 1 or 0.

NOTE: The default state for all logic pins is a logic one (1).

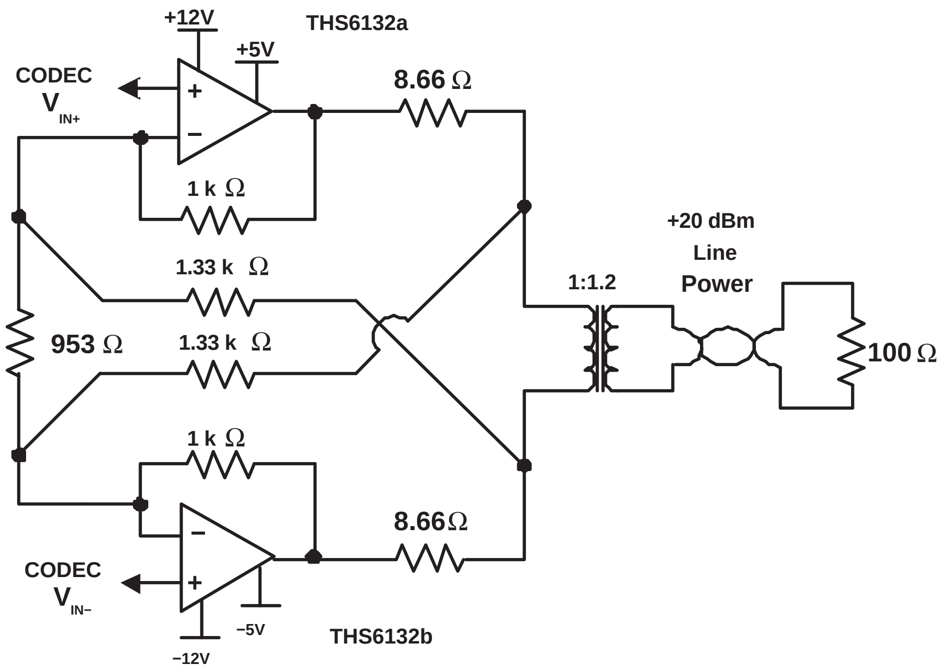
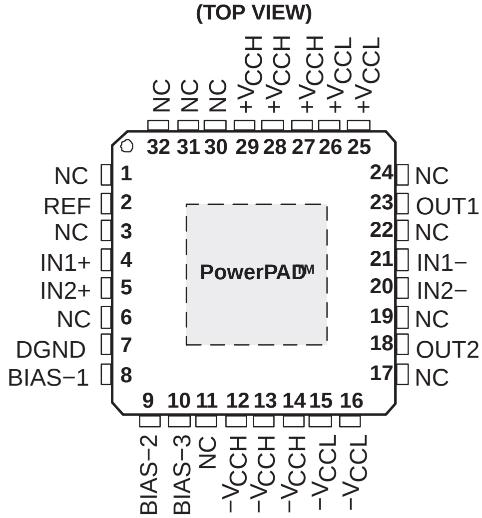


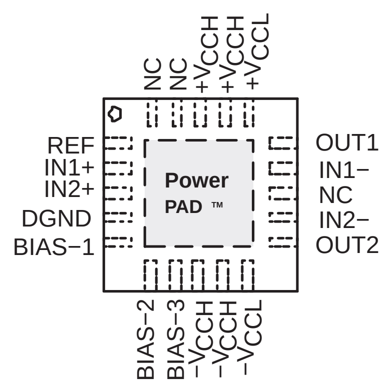
Figure 1. ±12 V Active Termination ADSL CO Line Driver Circuit (Synthesis Factor = 4; CF = 5.6)

PIN ASSIGNMENTS

THS6132
TQFP PowerPAD (VFP) PACKAGE
(TOP VIEW)



THS6132
Leadless 5X5 PowerPAD
(RGW) PACKAGE
(TOP VIEW)



TYPICAL CHARACTERISTICS

Table of Graphs

		FIGURE
Output voltage headroom	vs Output current	2
Common-mode rejection ratio	vs Frequency	3
Crosstalk	vs Frequency	4
Quiescent current	vs Temperature	5, 6
Large signal bandwidth	vs Frequency	7 − 10
Noise	vs Frequency	11
Overdrive recovery		12
Power supply rejection ratio	vs Frequency	13
Small signal frequency response		14, 15, 16
Small signal bandwidth	vs Frequency	17 − 28
Slew rate	vs Output voltage	29
Closed-loop output impedance	vs Frequency	30, 31
Shutdown response		32
Common-mode rejection ratio	vs Common-mode input voltage	33
Input bias current	vs Temperature	34
Input offset voltage	vs Temperature	35
Current draw distribution	vs Output voltage	36, 37
Output voltage	vs Temperature	38
Differential distortion	vs Frequency	39 − 52
Differential distortion	vs Differential output voltage	53 − 63
Single ended distortion	vs Frequency	64, 65

OUTPUT VOLTAGE HEADROOM vs OUTPUT CURRENT

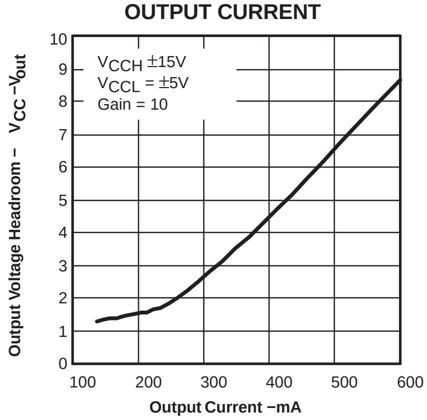


Figure 2

COMMON-MODE REJECTION RATIO vs FREQUENCY

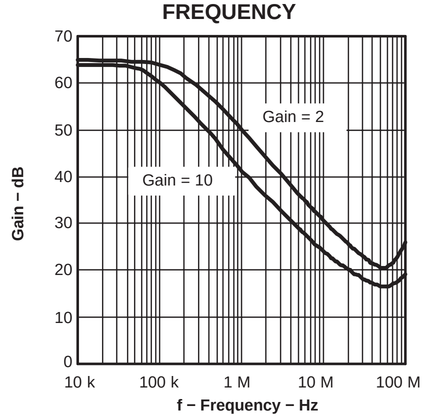


Figure 3

CROSSTALK vs FREQUENCY

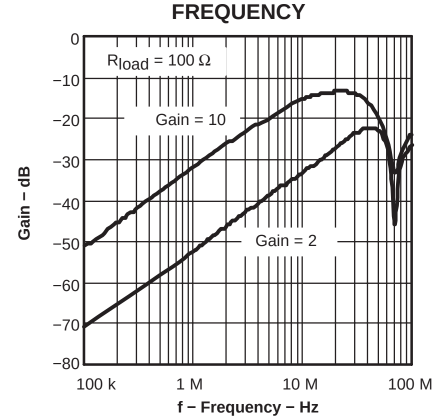


Figure 4

QUIESCENT CURRENT vs TEMPERATURE

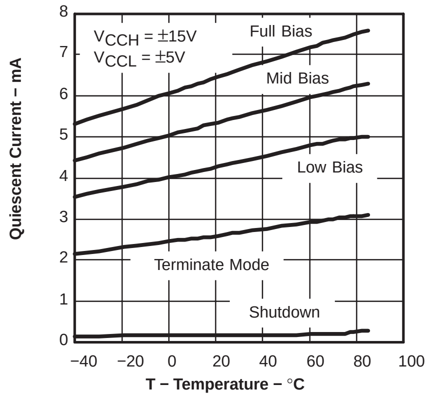


Figure 5

QUIESCENT CURRENT vs TEMPERATURE

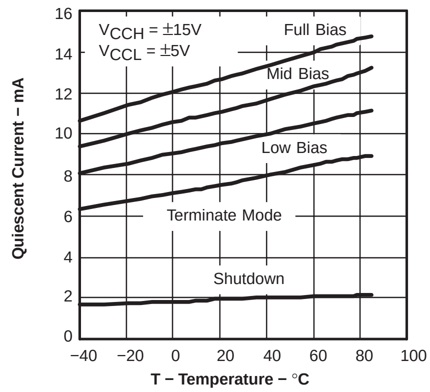


Figure 6

LARGE SIGNAL BANDWIDTH vs FREQUENCY

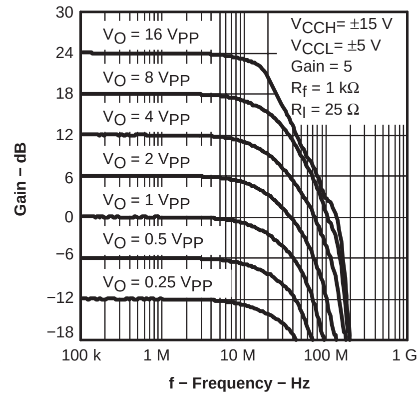


Figure 7

LARGE SIGNAL BANDWIDTH vs FREQUENCY

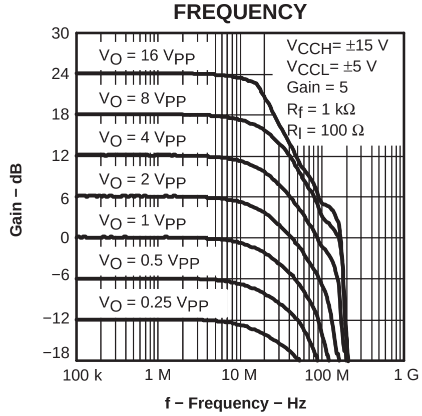


Figure 8

LARGE SIGNAL BANDWIDTH vs FREQUENCY

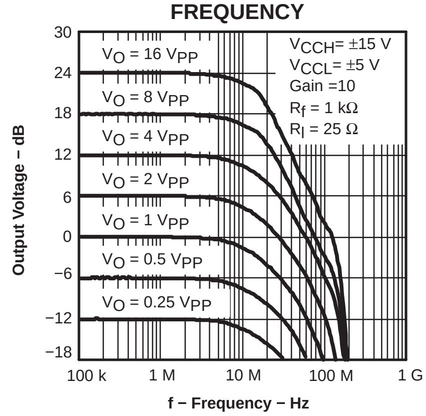


Figure 9

LARGE SIGNAL BANDWIDTH vs FREQUENCY

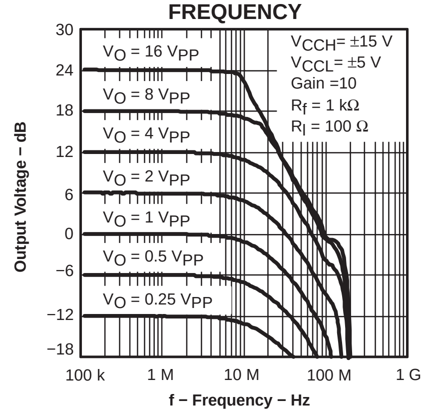


Figure 10

NOISE vs FREQUENCY

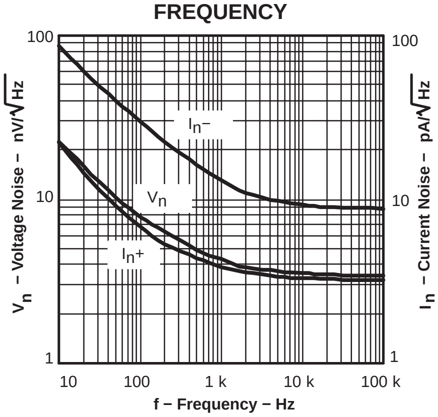


Figure 11

OVERDRIVE RECOVERY

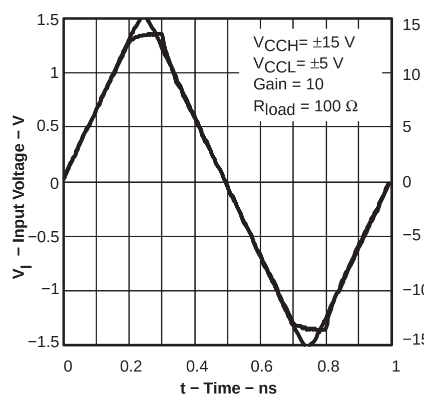


Figure 12

POWER SUPPLY REJECTION RATIO vs FREQUENCY

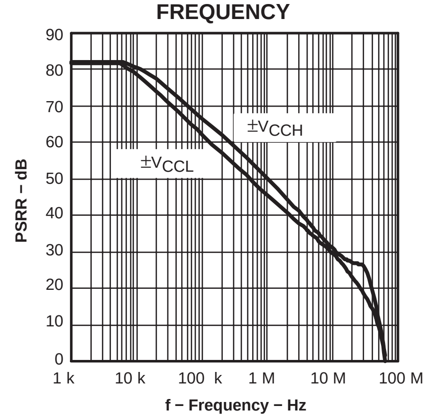


Figure 13

SMALL SIGNAL FREQUENCY RESPONSE

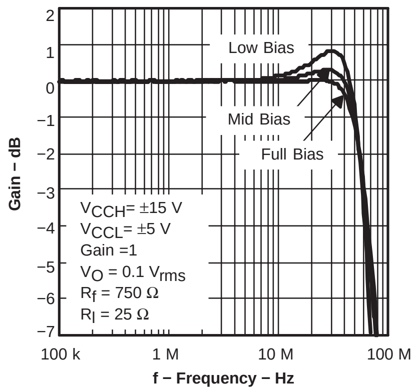


Figure 14

SMALL SIGNAL FREQUENCY RESPONSE

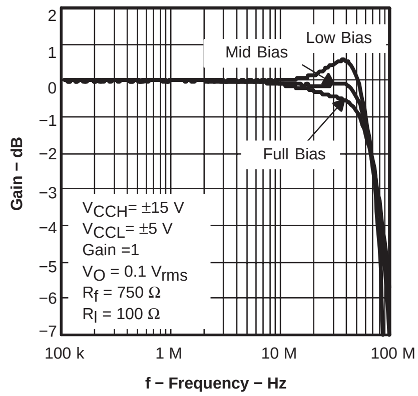


Figure 15

SMALL SIGNAL FREQUENCY RESPONSE

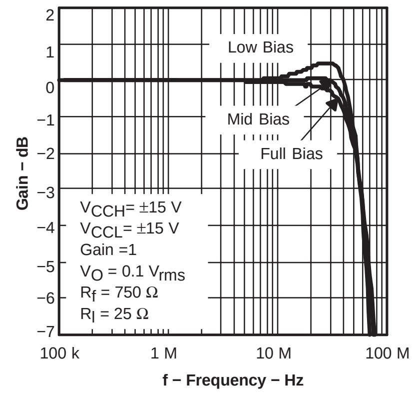


Figure 16

SMALL SIGNAL BANDWIDTH vs FREQUENCY

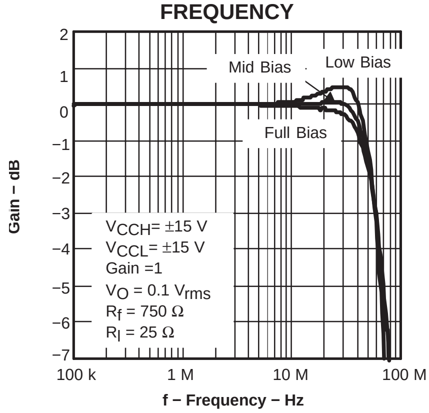


Figure 17

SMALL SIGNAL BANDWIDTH vs FREQUENCY

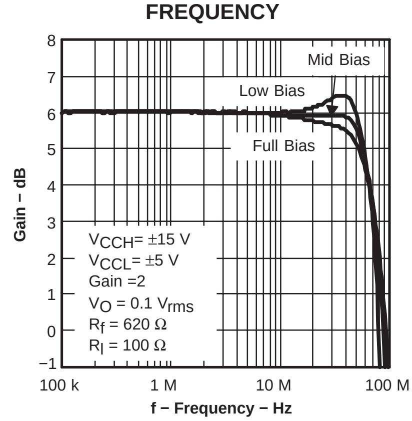


Figure 18

SMALL SIGNAL BANDWIDTH vs FREQUENCY

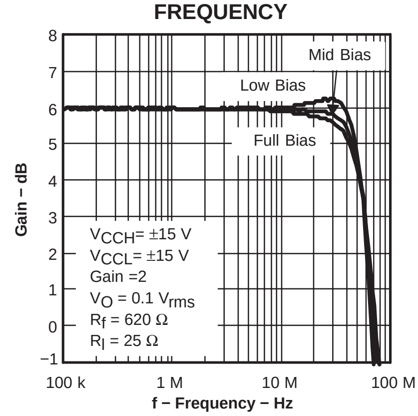


Figure 19

SMALL SIGNAL BANDWIDTH vs FREQUENCY

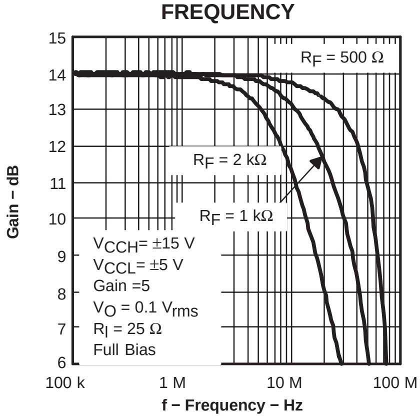


Figure 20

SMALL SIGNAL BANDWIDTH vs FREQUENCY

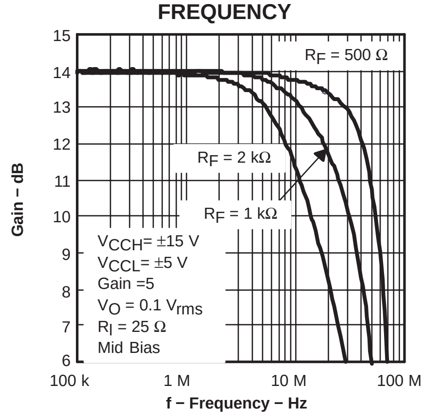


Figure 21

SMALL SIGNAL BANDWIDTH vs FREQUENCY

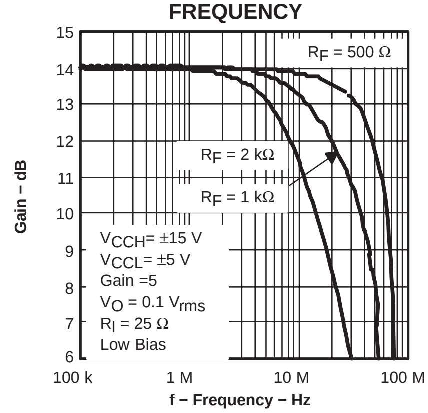


Figure 22

SMALL SIGNAL BANDWIDTH vs FREQUENCY

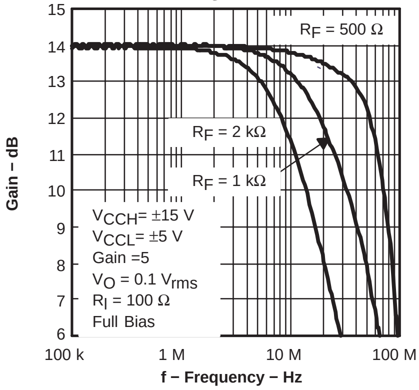


Figure 23

SMALL SIGNAL BANDWIDTH vs FREQUENCY

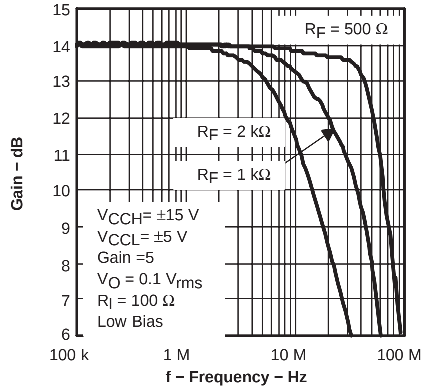


Figure 24

SMALL SIGNAL BANDWIDTH vs FREQUENCY

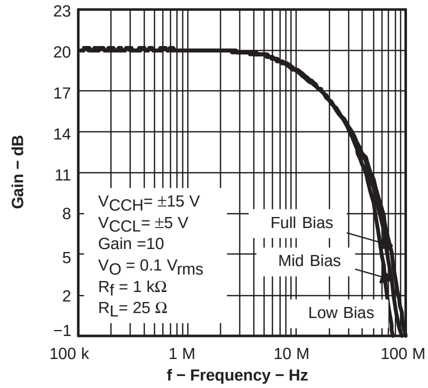


Figure 25

SMALL SIGNAL BANDWIDTH vs FREQUENCY

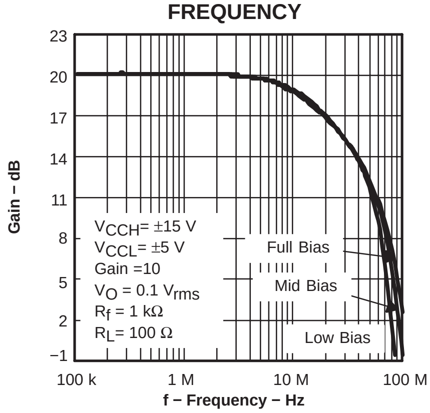


Figure 26

SMALL SIGNAL BANDWIDTH vs FREQUENCY

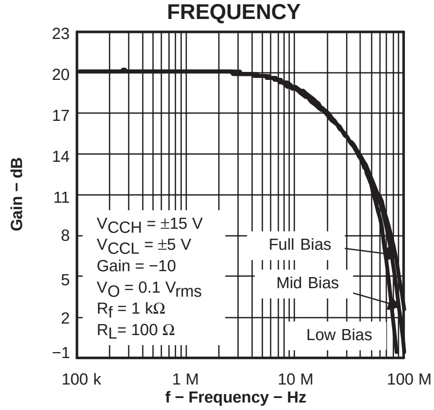


Figure 27

SMALL SIGNAL BANDWIDTH vs FREQUENCY

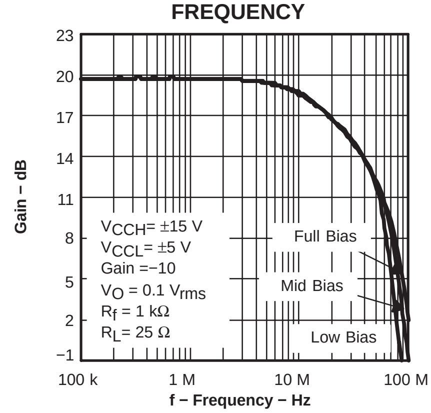


Figure 28

SLEW RATE vs OUTPUT VOLTAGE

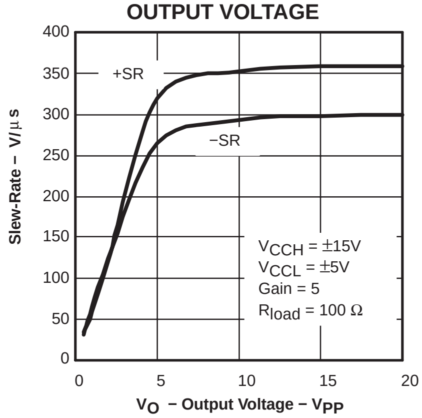


Figure 29

CLOSED LOOP OUTPUT IMPEDANCE vs FREQUENCY

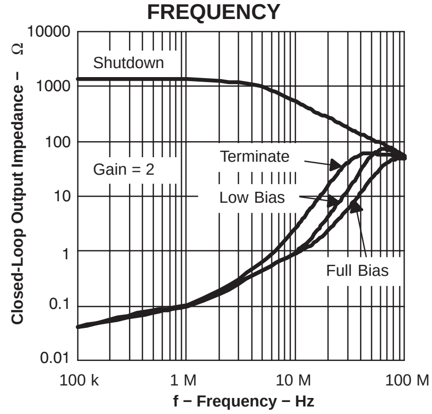


Figure 30

CLOSED LOOP OUTPUT IMPEDANCE vs FREQUENCY

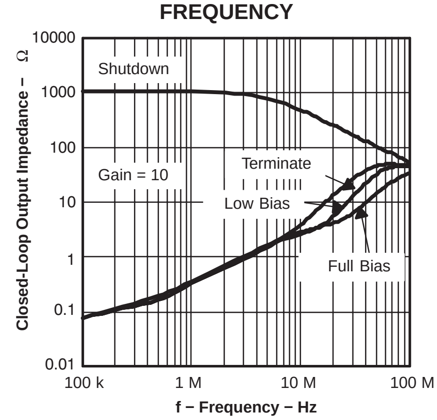


Figure 31

SHUTDOWN RESPONSE

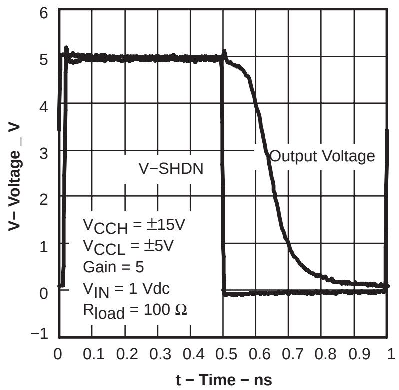


Figure 32

COMMON-MODE REJECTION RATIO vs COMMON-MODE INPUT VOLTAGE

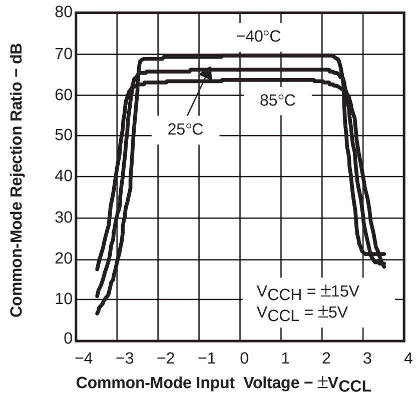


Figure 33

INPUT BIAS CURRENT vs TEMPERATURE

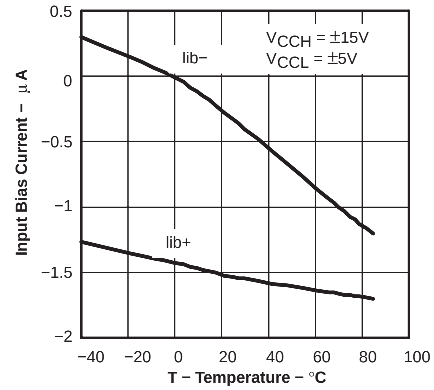


Figure 34

INPUT OFFSET VOLTAGE vs TEMPERATURE

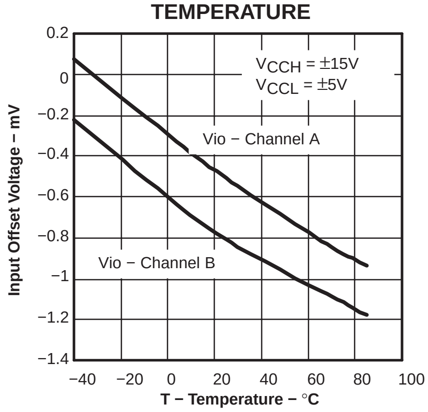


Figure 35

CURRENT DRAW DISTRIBUTION vs OUTPUT VOLTAGE

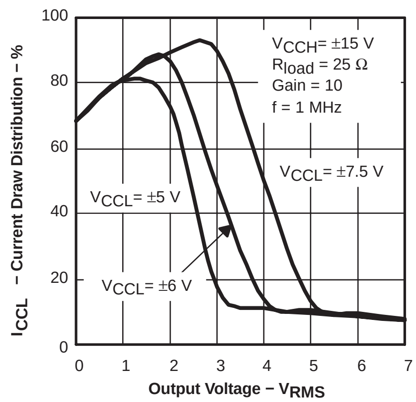


Figure 36

CURRENT DRAW DISTRIBUTION vs OUTPUT VOLTAGE

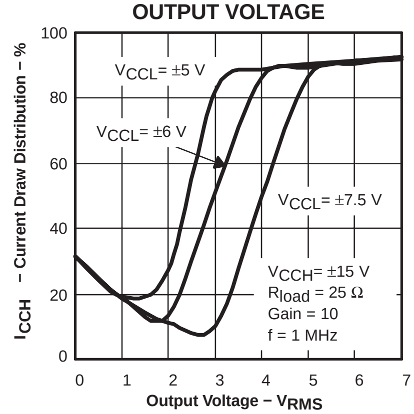


Figure 37

OUTPUT VOLTAGE vs TEMPERATURE

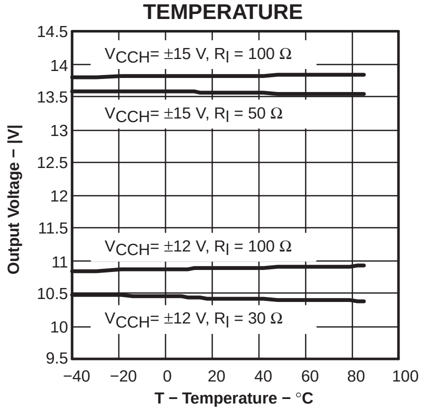


Figure 38

DIFFERENTIAL DISTORTION vs FREQUENCY

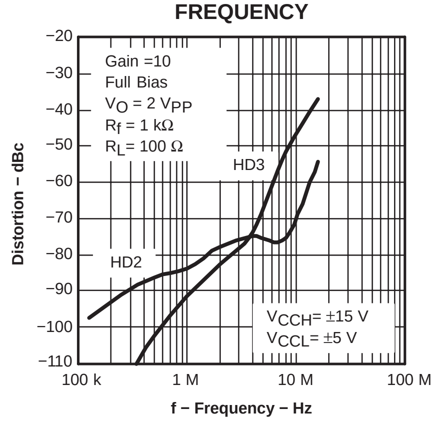


Figure 39

DIFFERENTIAL DISTORTION vs FREQUENCY

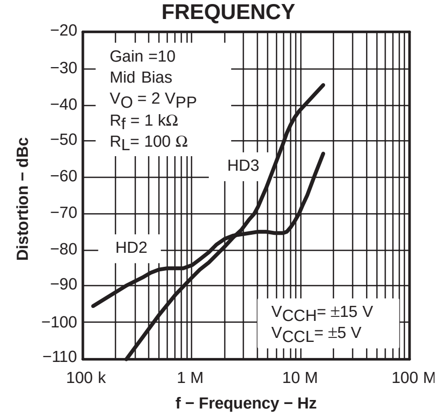


Figure 40

DIFFERENTIAL DISTORTION vs FREQUENCY

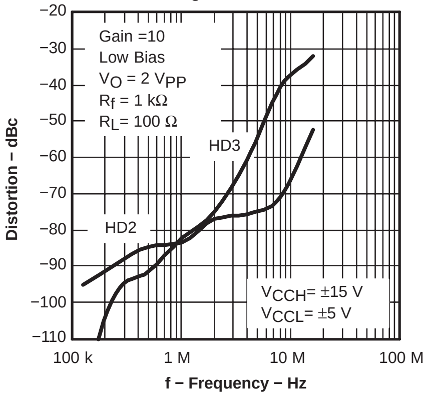


Figure 41

DIFFERENTIAL DISTORTION vs FREQUENCY

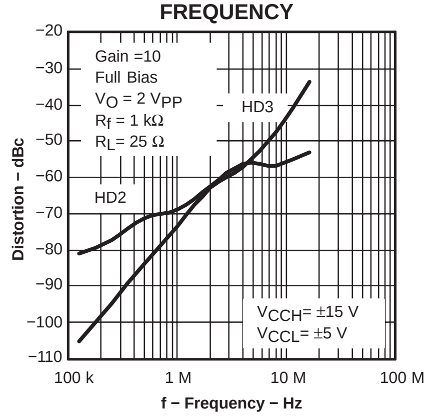


Figure 42

DIFFERENTIAL DISTORTION vs FREQUENCY

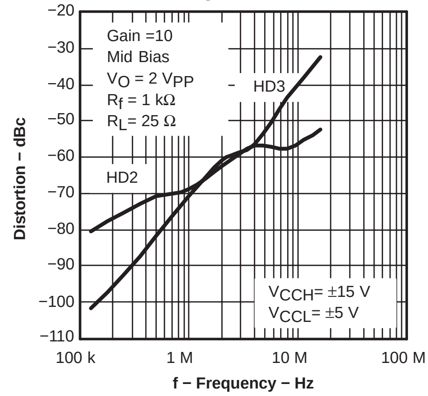


Figure 43

DIFFERENTIAL DISTORTION vs FREQUENCY

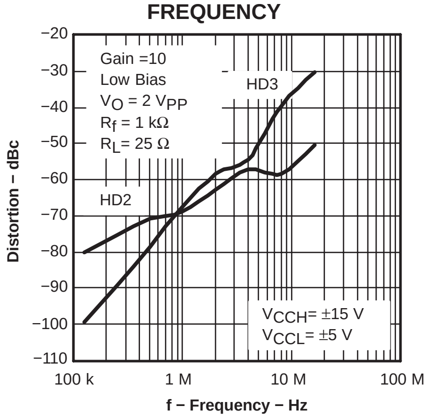


Figure 44

DIFFERENTIAL DISTORTION vs FREQUENCY

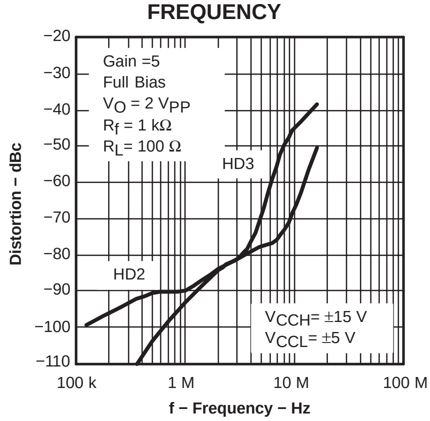


Figure 45

DIFFERENTIAL DISTORTION vs FREQUENCY

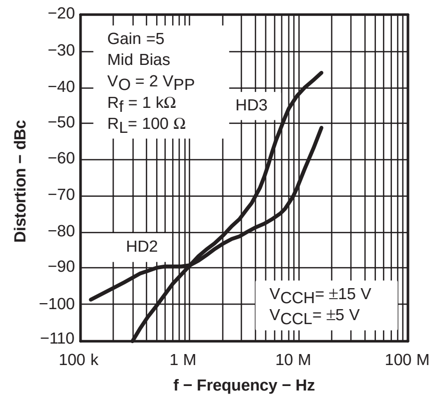


Figure 46

DIFFERENTIAL DISTORTION vs FREQUENCY

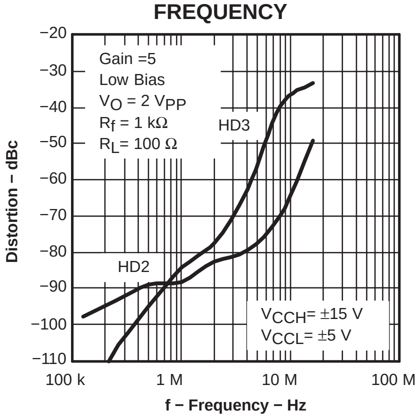


Figure 47

DIFFERENTIAL DISTORTION vs FREQUENCY

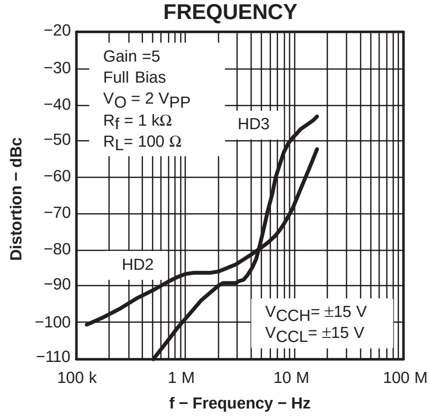


Figure 48

DIFFERENTIAL DISTORTION vs FREQUENCY

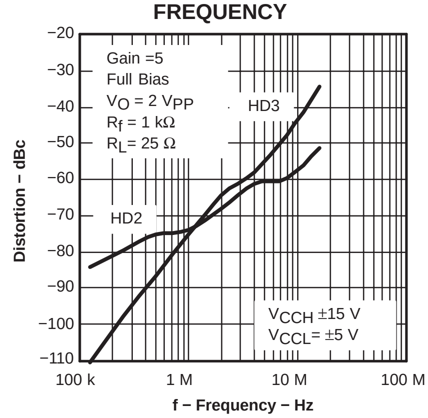


Figure 49

DIFFERENTIAL DISTORTION vs FREQUENCY

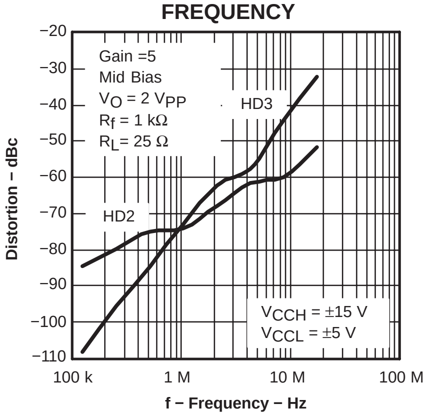


Figure 50

DIFFERENTIAL DISTORTION vs FREQUENCY

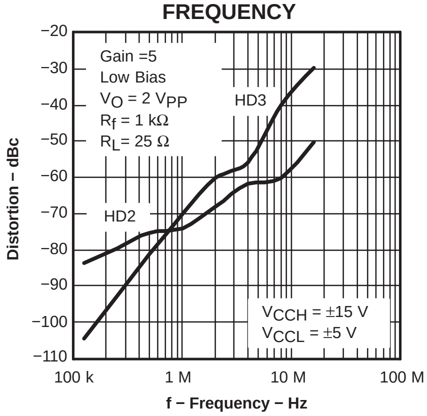


Figure 51

DIFFERENTIAL DISTORTION vs FREQUENCY

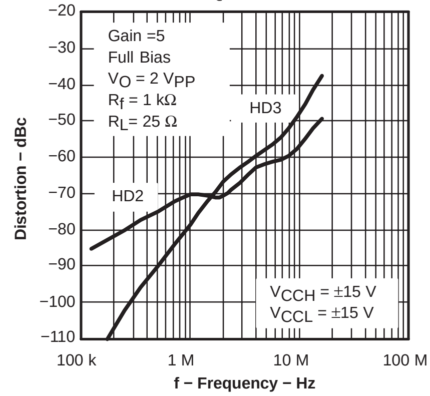


Figure 52

DIFFERENTIAL DISTORTION vs DIFFERENTIAL OUTPUT VOLTAGE

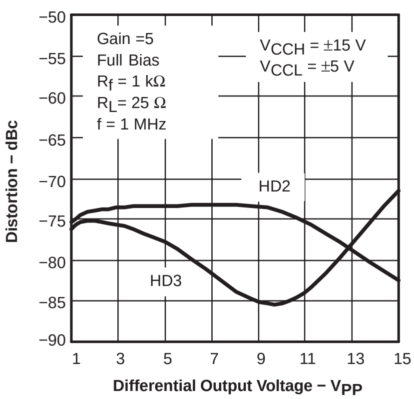


Figure 53

DIFFERENTIAL DISTORTION vs DIFFERENTIAL OUTPUT VOLTAGE

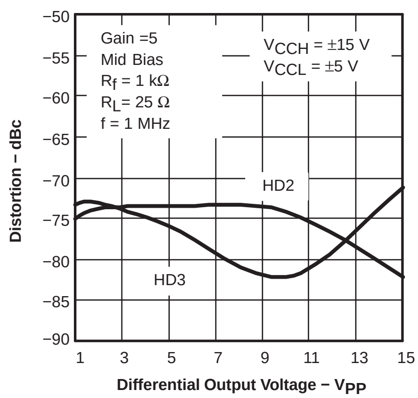


Figure 54

DIFFERENTIAL DISTORTION vs DIFFERENTIAL OUTPUT VOLTAGE

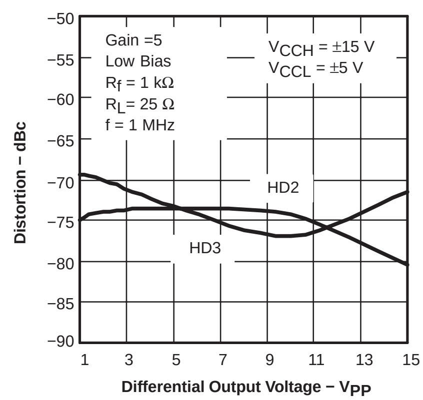


Figure 55

DIFFERENTIAL DISTORTION vs DIFFERENTIAL OUTPUT VOLTAGE

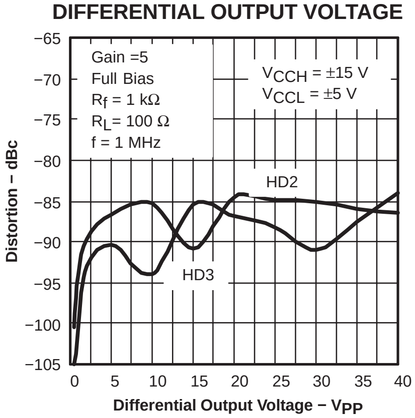


Figure 56

DIFFERENTIAL DISTORTION vs DIFFERENTIAL OUTPUT VOLTAGE

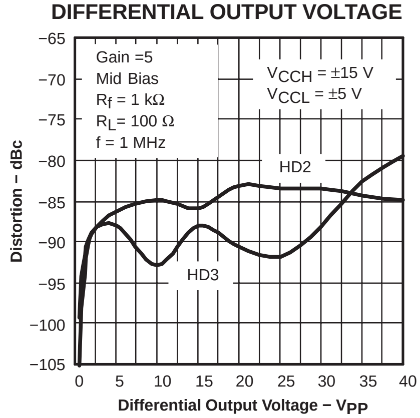


Figure 57

DIFFERENTIAL DISTORTION vs DIFFERENTIAL OUTPUT VOLTAGE

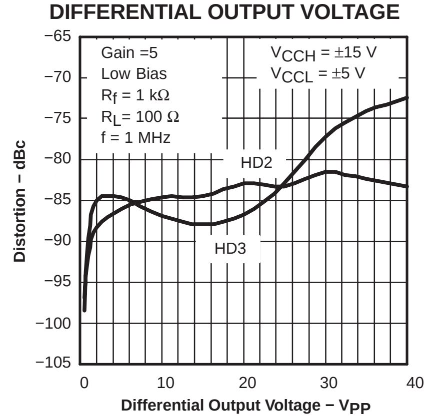


Figure 58

DIFFERENTIAL DISTORTION
vs
DIFFERENTIAL OUTPUT VOLTAGE

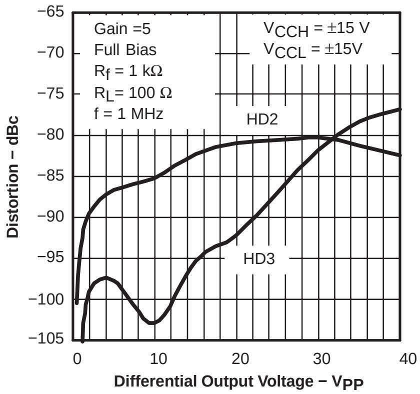


Figure 59

DIFFERENTIAL DISTORTION
vs
DIFFERENTIAL OUTPUT VOLTAGE

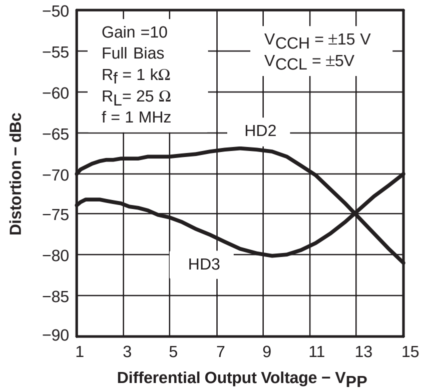


Figure 60

DIFFERENTIAL DISTORTION
vs
DIFFERENTIAL OUTPUT VOLTAGE

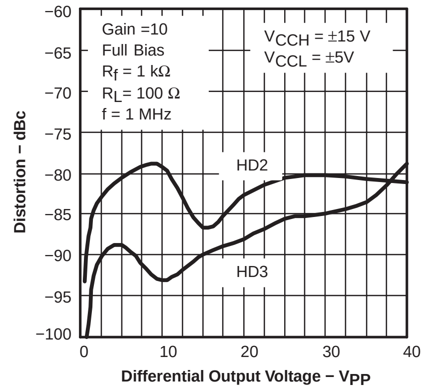


Figure 61

DIFFERENTIAL DISTORTION
vs
DIFFERENTIAL OUTPUT VOLTAGE

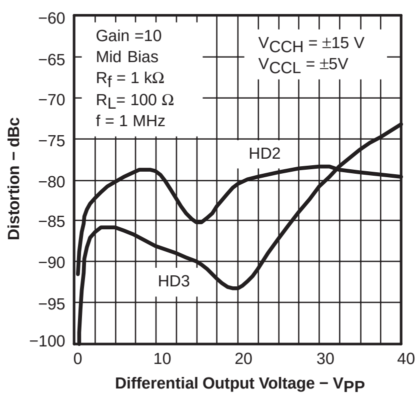


Figure 62

DIFFERENTIAL DISTORTION
vs
DIFFERENTIAL OUTPUT VOLTAGE

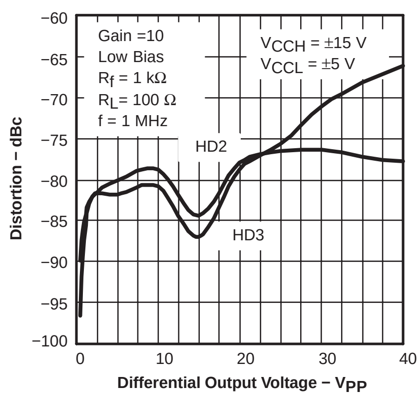


Figure 63

SINGLE ENDED DISTORTION
vs
FREQUENCY

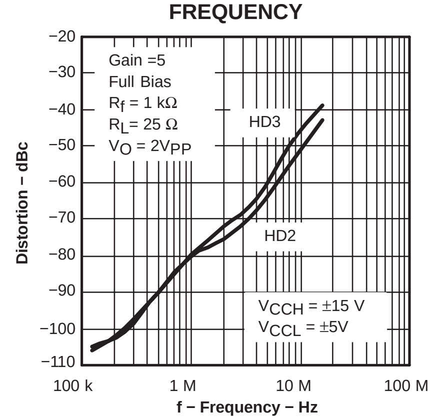


Figure 64

SINGLE ENDED DISTORTION
vs
FREQUENCY

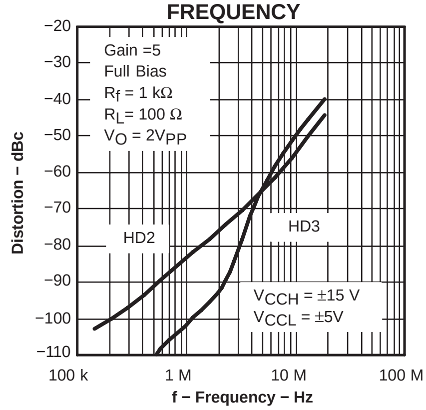


Figure 65

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
THS6132VFP	ACTIVE	HLQFP	VFP	32	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	THS6132	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

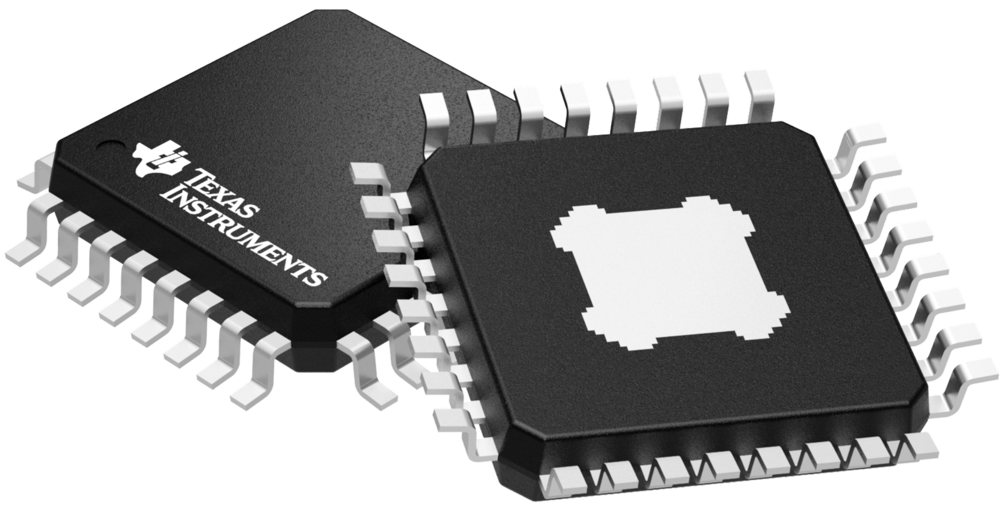
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

VFP 32 PowerPAD™ LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4200791/D

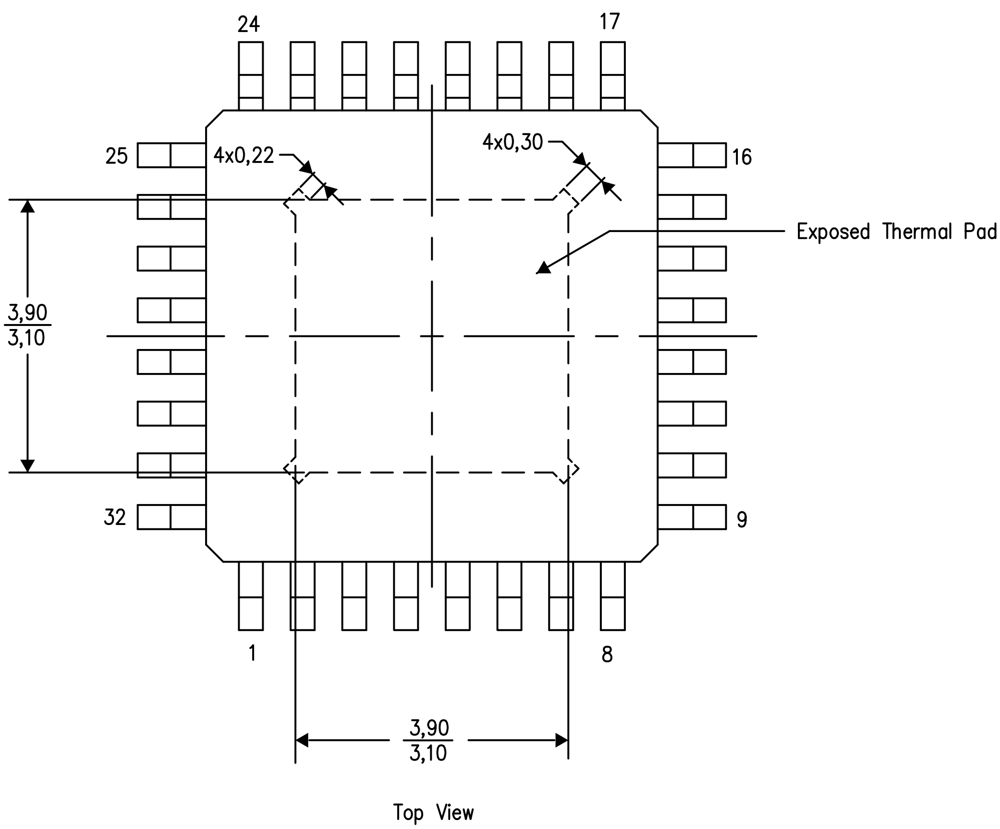
VFP (S-PQFP-G32) PowerPAD™ PLASTIC QUAD FLATPACK

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

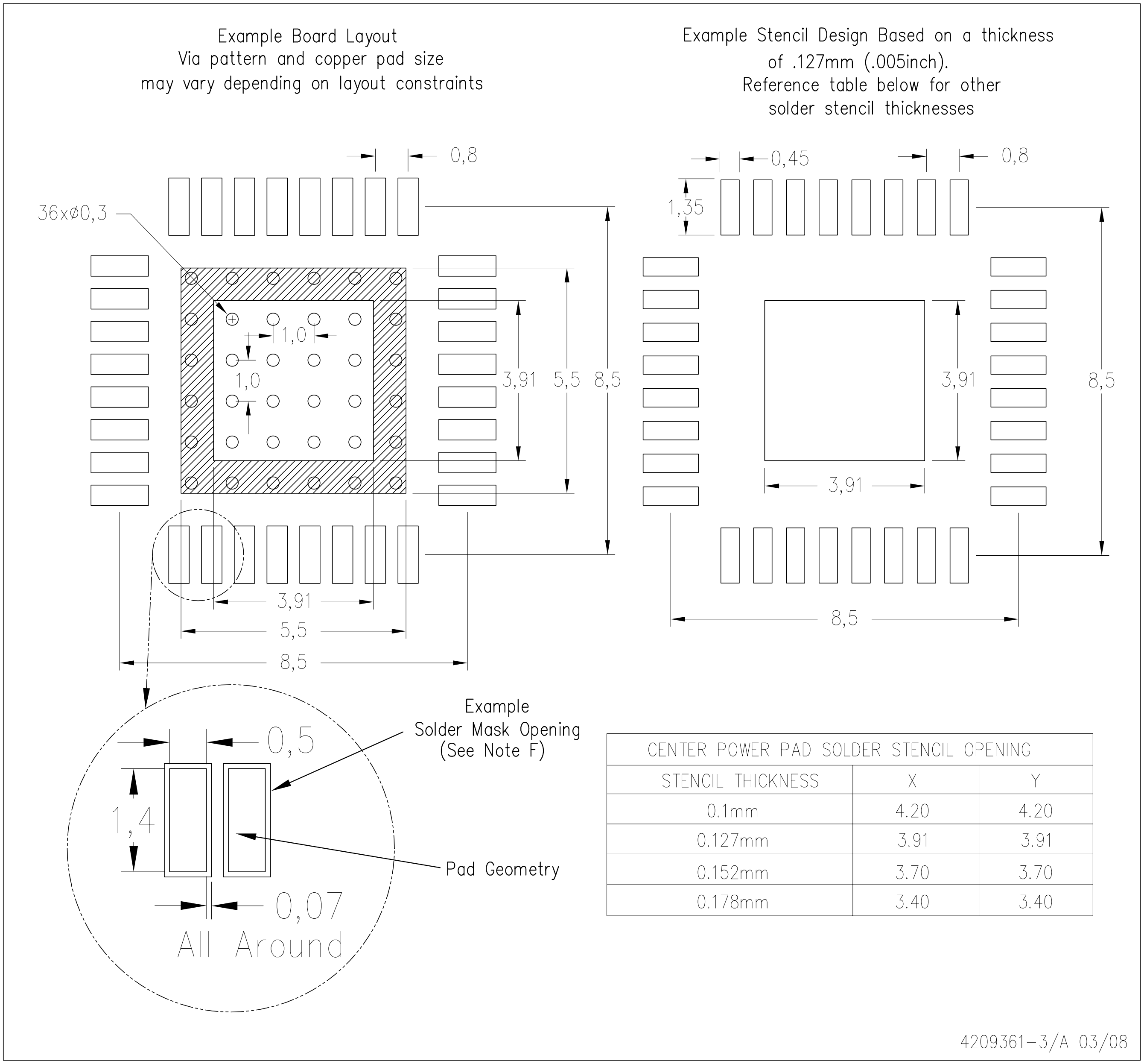


Exposed Thermal Pad Dimensions

4206318-2/E 06/13

NOTE: All linear dimensions are in millimeters

VFP (S–PQFP–G32) PowerPAD™



CENTER POWER PAD SOLDER STENCIL OPENING		
STENCIL THICKNESS	X	Y
0.1mm	4.20	4.20
0.127mm	3.91	3.91
0.152mm	3.70	3.70
0.178mm	3.40	3.40

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE AND DISCLAIMER